



Analogue circuit realisation of surface-confined redox reaction kinetics

M.K. Tageldeen^a, I. Pagkalos^a, S.S. Ghoreishizadeh^b, E.M. Drakakis^{a,*}

^a Bioinspired VLSI Circuits and Systems Group, Department of Bioengineering, Imperial College London, Exhibition Road, London, SW7 2AZ, UK

^b Department of Electronic and Electrical Engineering, University College London, Malet Place, London, WC1E 7JE, UK

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ABSTRACT

The literature on voltammetry and electrochemical impedance spectroscopy (EIS) recognises the importance of using large-amplitude sinusoidal perturbations to better characterise electrochemical systems. To identify the parameters of a given reaction, various electrochemical models with different sets of values are simulated and compared against the experimental data to determine the best-fit set of parameters. However, the process of solving these nonlinear models is computationally expensive. This paper proposes analogue circuit elements for synthesising surface-confined electrochemical kinetics at the electrode interface. The resultant analogue model could be used as a solver to compute reaction parameters as well as a tracker for ideal biosensor behaviour. The performance of the analogue model was verified against numerical solutions to theoretical and experimental electrochemical models. Results show that the proposed analogue model has a high accuracy of at least 97% and a wide bandwidth of up to 2 kHz. The circuit consumed an average power of 9 μ W.

1. Introduction

Surface-confined redox reactions are chemical redox reactions in which both the reduced and oxidized moieties are tightly bound to the electrode surface. These reactions have gained a lot of attention over the last few decades due to the advances in the development of chemically modified electrode surfaces (Mayall et al., 2020; Lyons, 2002).

Characterizing surface-confined redox reactions plays an important role in many fields, including sensor design (Gonzalez and Sequí-Castellano, 2021), energy storage and generation (Braun, 2018), synthetic electrochemistry (Yan et al., 2017), biological mechanisms modelling (Jenner and Butt, 2018) and the study of proteins through protein films (Huang et al., 2008). In biosensing, for example, chemical detection is accomplished by sensing the changes of the electrochemical reaction parameters as a result of introducing the measured species on the electrode; hence, identifying the process parameters is critical for sensor calibration and optimal performance (Sun, 2008).

Different models can be used to fit the measured data and infer the chemical parameters depending on the electrochemical process considered. These chemical models are generally described by equivalent electrical circuits that include, at least, an impedance element to model the electron transfer from the reduced to the oxidized species and a capacitors element to model the double layer capacitance that arises from the formation of two layers of opposing charges on the electrode

interface (Freeborn et al., 2014; Cao et al., 2010; Fasmin and Srinivasan, 2017).

Voltammetry is a key technique for the characterization of electrochemical reaction parameters at the electrode interface. Through the application of a time-varying voltage, the resultant current can be analysed to identify process parameters such as the kinetic rate constant and the electron transfer coefficient (Bell, Anastassiou, O'Hare, Parker and Siggers, 2011). When the applied voltage is measured in reference to the redox formal potential (i.e. where the reaction is in equilibrium), it is referred to as the over-potential (E^*). Fig. 1 shows the input voltage profiles for three different types of voltammetry; namely cyclic voltammetry (Fig. 1a), pure sinusoidal voltammetry (Fig. 1b) and AC voltammetry (Fig. 1c). AC voltammetry can be seen as a combination of the other two types, where E_{ac}^* will be used to refer to the slow potential sweep in cyclic voltammetry, and E_{ac}^* will refer to the sinusoidal perturbation.

Cyclic voltammetry performs poorly when the response current is dominated by the charging current due to the double-layer capacitance current (Bard and Faulkner, 2001). AC voltammetry coupled with Fourier transform performs significantly better as it allows the isolation of the background charging current and provides insights about the chemical processes in higher harmonic frequencies (Bond, 1980; Guo et al., 2004). Traditionally, AC voltammetry is carried out by applying a small-amplitude sinusoidal perturbation (E_{ac}^*), between 2 and 10 mV,

* Corresponding author.

E-mail address: e.drakakis@imperial.ac.uk (E.M. Drakakis).

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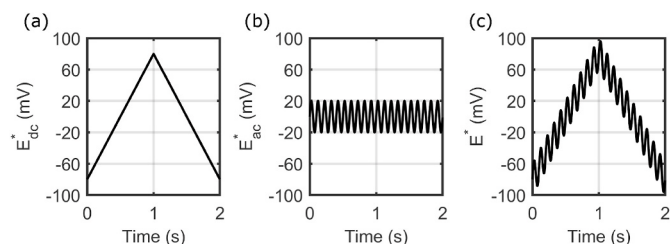


Fig. 1. Over-potential (E^*) vs time for three voltammetry types: (a) cyclic voltammetry, (b) sinusoidal voltammetry and (c) AC voltammetry.

superimposed on a linear sweep (E_{dc}^*). Fourier transform is then used to extract the DC, fundamental and harmonic components of the total measured current. The contribution of the capacitance current to the second and higher components is minimal; however, small-amplitude AC voltammetry produces small current harmonics which are difficult to extract and measure (Bond, 1980; Guo et al., 2004). Large-amplitude and square wave voltammetry address this issue and produce easily measurable harmonics with high current-to-background ratio (Guo et al., 2004; Zhang et al., 2005).

Electrochemical Impedance Spectroscopy (EIS) is another method widely used for studying electrode-electrolyte interface kinetics (Sun, 2008). It is closely related to small-amplitude sinusoidal voltammetry, but the frequency of the input signal is swept over a wide range. EIS offers significant advantages in terms of improved sensitivity and lower limit of detection (LoD) when compared with other methods such as amperometry (Li et al., 2021; Sun, 2008). Additionally, with impedance methods, processes of varying time constants can be studied and analysed. Similar to the trends in voltammetry, there is a growing interest in the application of large input signals to study nonlinear reaction kinetics, in what is known as nonlinear electrochemical impedance spectroscopy (NLEIS) (Fasmin and Srinivasan, 2017).

A major challenge in inferring reaction parameters from potential-current measurements is the unavailability of a general analytical solution to the reaction model. This is especially the case when nonlinear harmonic responses are considered. There are analytical solutions reported in the literature but they are limited to specific input potential functions such as pure sinusoidal voltammetry (Bell et al., 2011). An alternative approach is to use numerical simulations to solve the inverse problem: many numerical simulations with different sets of parameter values are produced and compared against the experimental data, then the set of parameters with the smallest error is chosen (Lloyd-Laney et al., 2021). However, this approach is power demanding and computationally expensive (Lloyd-Laney et al., 2021). Approximation methods could be used to improve the computation speed but may lead to reduced accuracy, and impose constraints on the applied potential signal. The availability of an analogue chip that mimics the physical dynamic of surface-confined reactions has the potential of accelerating parameters estimation and reducing power consumption considerably by replacing numerical simulations.

The analogue realisation of models describing the electrochemical interface kinetics offers a number of benefits: (1) By comparing the analogue model with an actual sensor, an estimation of the sensor drift could be calculated and accounted for. This would allow using sensors for extended time periods and would reduce the frequency of calibration. (2) A reconfigurable chip that can be programmed to simulate various reactions would accelerate computing reaction parameters with lower power and higher throughput in comparison with numerical approximations. (3) The analogue model can improve medical implants by offering the capability to predict their behaviour before they are surgically placed inside patients; this is similar to the work by Scott and Single (2014).

In this article, we present novel elements for the analogue synthesis of chemical models describing surface-confined redox reactions. In

general, our faradaic (electron transfer) model is accurate, does not make any approximations on the BV equation and does not depend on memristors which can be challenging to fabricate and characterise. The blocks presented here are limited to modelling surface-confined quasi-reversible redox reactions and the discussion focuses on AC voltammetry. Finally, this paper validates the approach and elements using simulations.

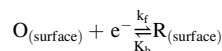
2. Theory

The Randles circuit is a widely used model for the electrode interface (Fouquet et al., 2006; Sabatier et al., 2006; Cao et al., 2010). For surface-confined redox reactions, the equivalent Randles circuit (Zhang et al., 2005; Guo et al., 2004) is shown in Fig. 2, and it consists of an electrolyte resistance (R_S) that is connected in series with the parallel combination of a double layer capacitance (C_{dl}) and a faradaic impedance (Z_F).

When a potential difference is applied across the circuit in Fig. 2, the total current is the summation of the faradaic current (I_F), through the faradaic branch, and the charging current (I_C) due to the double-layer capacitance (C_{dl}):

$$I = I_F + I_C \quad (1)$$

For surface-confined reactions, the solution resistance (R_S) has a value in the tenth of Ohms and thus can be neglected (Zhang et al., 2005). The faradaic impedance (Z_F), due to the electron transfer between the redox partners, is the most important part of the model. Given the following one-electron surface-confined quasi-reversible redox reaction:



Where O and R are the surface-confined oxidized and reduced species, and the quantities k_f (s^{-1}), k_b (s^{-1}) represent the forward and backward electron transfer rate constants respectively, as shown in Fig. 3a. Fig. 3b shows that when applying an over-potential to the electrode, electrons are either sourced from or sinked into the electrode depending on whether the species are oxidized or reduced.

The most popular model for describing the relation between the electron transfer current and the applied over-potential on the electrode is the Butler-Volmer (BV) equation (Noren and Hoffman, 2005; McAdams and Jossinet, 2000). According to the BV formalism, the faradaic current for a surface-confined redox reaction is given by (Guo et al., 2004; Bell et al., 2011).

$$I_F = FA\Gamma\dot{\theta} = FA\Gamma[k_b(1 - \theta) - k_f\theta] \quad (2)$$

Where F is the Faraday constant ($96485.3 \text{ C mol}^{-1}$), A is the area of the electrode (m^2), Γ is the excess surface concentration for both the reduced and oxidized forms of the species (mol m^{-2}) and θ is the ratio between the electrode surface that is covered by the oxidized species and the total area. Fig. 3 details how the excess concentration and the fractional coverage are calculated. The quantities k_f , k_b are given by the

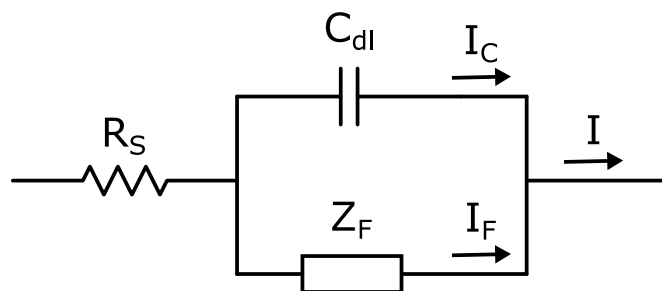


Fig. 2. Equivalent Randles circuit of a surface-confined redox reaction.

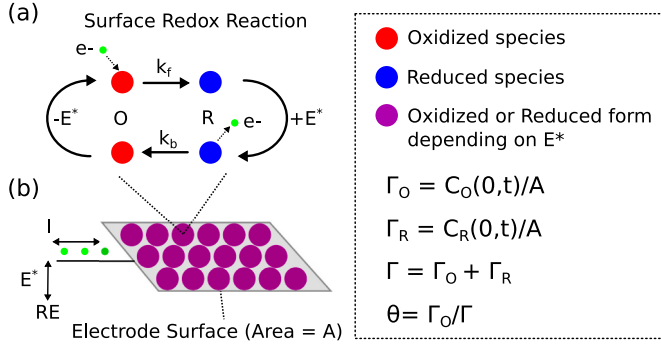


Fig. 3. Surface confined redox reaction: (a) a single electron transfer between the reduced and oxidized species (b) current flow in/out the electrode when an over-potential is applied. A is the electrode area, $C_O(0, t)$ and $C_R(0, t)$ are the time-variant surface concentration of the redox partners. Γ_O is the excess concentration of oxidized species, Γ_R is the excess of reduced species, Γ is the total excess concentration, and θ is the fractional coverage of the oxidized species.

following equations:

$$k_f = k_0 e^{\frac{-\alpha F E^*}{R_g T}} \quad (3)$$

$$k_b = k_0 e^{\frac{(1-\alpha) F E^*}{R_g T}} \quad (4)$$

Where α is the electron transfer coefficient, k_0 (s^{-1}) is the standard electron transfer rate constant, $E^*(V)$ is the applied time-varying over-potential, R_g ($8.31 \text{ C V mol}^{-1} \text{ K}^{-1}$) is the universal gas constant and T (298.15 K) is the absolute temperature.

We define a normalised faradaic current (i_F) that relates to I_F through a non-dimensional scaling factor equal to $F A \Gamma / \hat{Q}$, where $\hat{Q} = 1 \text{ C}$. Hence, i_F is then expressed as the rate of change of θ (i.e. rate constant) times a unit charge $\hat{Q}$ according to equations (5) and (6):

$$I_F = \frac{F A \Gamma}{\hat{Q}} i_F \quad (5)$$

$$i_F = \hat{Q} \times \dot{\theta} \quad (6)$$

Substituting equations (3) and (4) in (2), the rate constant is expressed by the following relationship (Guo et al., 2004; Anastassiou et al., 2005):

$$\dot{\theta} = k_0 e^{\frac{(1-\alpha) F E^*}{R_g T}} (1 - \theta) - k_0 e^{\frac{-\alpha F E^*}{R_g T}} \theta \quad (7)$$

Through further simplification, equation (7) can be rewritten as a first-order differential equation (DE).

$$\dot{\theta} + k_0 \left[e^{\frac{(1-\alpha) F E^*}{R_g T}} + e^{\frac{-\alpha F E^*}{R_g T}} \right] \theta = k_0 e^{\frac{(1-\alpha) F E^*}{R_g T}} \quad (8)$$

As mentioned previously, an analytical solution is available for DE (8) only for particular time-varying functions of E^* .

Continuing our discussion of the equivalent circuit model, the non-faradaic current (I_C) depends on the applied potential and the double-layer capacitance as seen in Fig. 2. This capacitance is due to the electrode and the electrolyte (redox partner) giving rise to layers of opposing charge. Several studies have shown that the double-layer capacitance (C_{dl}) is more accurately modelled as a fractional-order capacitor or a constant phase element (CPE) than an ideal capacitor (McAdams et al., 1995). Similar to our treatment of the faradaic current, we define a normalised charging current i_C according to the following relationship:

$$i_C = \frac{\hat{Q}}{F A \Gamma} C_{dl} \frac{dE}{dt} \quad (9)$$

3. Circuit realisation

In this section, we describe two different elements to model scaled values of the Z_F and C_{dl} respectively. Our approach simplifies the synthesis process significantly and affords the flexibility to realise different reaction models.

3.1. Modelling the faradaic impedance

First, we focus on the top-level block diagram shown in Fig. 4. Overall, the proposed element can be seen as a two-terminal component that physically emulates the faradaic impedance, or rather a scaled version of it ($\hat{Z}_F$), and directly fits into the circuit shown in Fig. 2. To that end, our proposed electrical component is designed to be bidirectional. In other words, both terminals can source and sink currents.

3.1.1. Bernoulli cell block

The objective of re-formulating the BV model into DE (8) is to allow systematic synthesis using familiar translinear circuits and simple amplifier topologies. The main circuit element in our synthesis approach is the Bernoulli cell (BC), which - in its linearised form - is used as a solver for DEs with the following formalism (Drakakis et al., 1999):

$$n C V_T \dot{w}(t) + I_u(t) w(t) = I_{IN}(t) \quad (10)$$

The schematics of the BC block is shown in Fig. 5 and the BC is emphasised with the red line in the same figure. When setting the ratio ($I_\theta(t)/I_Q$) to the variable $w(t)$, equation (10) can be derived from the BC block schematic by analysing the translinear loop, and by expressing the capacitor current as the derivative of the voltage at the source of the transistor in the BC (M3 in Fig. 5). The full analysis is provided by Drakakis et al. (1999). For brevity, we will drop the independent variable (t) when expressing time-varying currents from this point onwards. We now use the approach defined by Drakakis et al. (1999) to map the BV parameters onto equivalent electrical variables:

$$k_0 = \frac{I_0}{n C V_T} \quad (11)$$

$$V_T = \frac{R_g T}{F} \quad (12)$$

$$\theta = \frac{I_\theta}{I_Q} \quad (13)$$

$$i_F = \frac{I_\theta}{I_Q} \hat{Q} \quad (14)$$

Where C is the capacitor within the Bernoulli cell. Thus, the DE can be rewritten into the following electrical form:

$$\frac{\dot{I}_\theta}{I_Q} + \frac{I_U}{n C V_T} \frac{I_\theta}{I_Q} = \frac{I_{IN}}{n C V_T} \quad (15)$$

Where

$$I_U = I_0 \left[e^{\frac{(1-\alpha) V_{in}}{n V_T}} + e^{\frac{-\alpha V_{in}}{n V_T}} \right]$$

$$I_{IN} = I_0 e^{\frac{(1-\alpha) V_{in}}{n V_T}}$$

From (8) and (15), the applied input voltage (V_{in}) of the analogue circuit relates to the over-potential (E^*) through the following equation:

$$E^* = \frac{V_{in}}{n} \quad (16)$$

Where n is the subthreshold slope factor of the weakly inverted MOS transistors, which can take values from 1 to 1.5. Equation (16) is necessary to balance the n term in the denominator of the exponential term at the output of the utilized E+ cells (see Fig. 4).

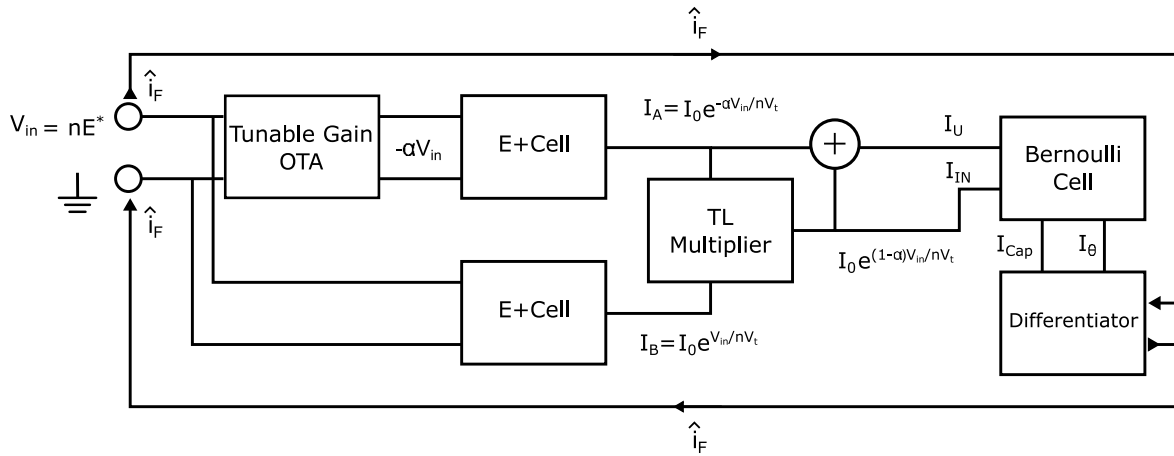


Fig. 4. Block diagram of the proposed two-terminal element which mimics surface-confined Butler-Volmer kinetics. The Bernoulli cell solves the Butler-Volmer differential equation.

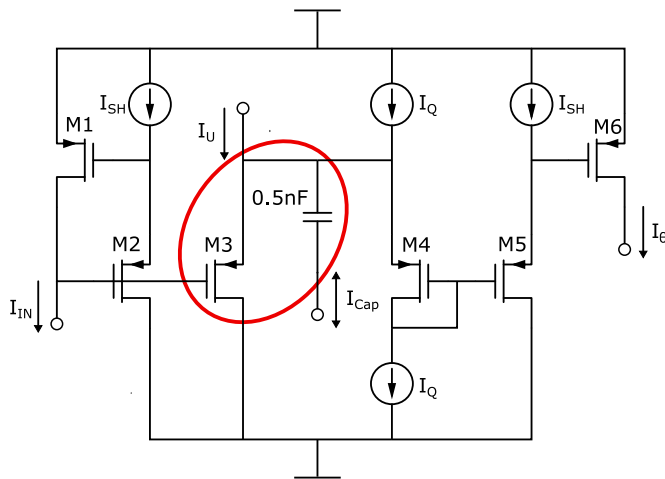


Fig. 5. Schematics of the BC block (Drakakis et al., 1999) mapped onto the BV variables. The BC is highlighted with the red circle.

As mentioned previously, the transistor-based BC approach can produce a solution to DE (15) - i.e. I_θ ; however, a current differentiator is needed to calculate the faradaic current according to equation (14). Finally, the rest of the blocks shown in Fig. 4 are needed to realise the current expressions feeding into the BC block; namely I_U and I_{IN} .

3.1.2. Tunable gain block

Firstly, we consider the multiplication of the electron transfer coefficient (α) and the input potential (V_{in}) that appears in the exponential terms of the DE. The circuit shown in Fig. 6 operates as a tunable gain block. This behaviour is achieved by converting the input voltage into

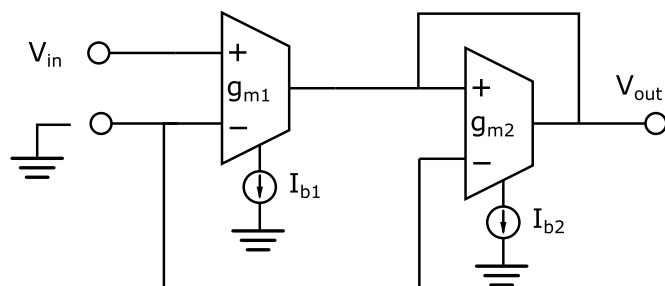


Fig. 6. Block diagram of the circuit used to implement the tunable gain stage.

current through the transconductance of the first OTA (g_{m1}). The second OTA, which is identical to the first one, is connected as an active resistor and reconverts the current from the first stage back into an output voltage through g_{m2} . Thus, the circuit scales the input voltage (V_{in}) by the transconductance ratio (g_{m1}/g_{m2}). While operating in weak inversion, the transconductance ratio of the two identical OTAs is equal to the ratio of their biasing currents (Tsividis, 2002). Hence, by modelling α as the ratio between the two biasing currents I_{b1}/I_{b2} , the multiplication term ($-\alpha V_{in}$) is equal to the output voltage of the block:

$$V_{out} = -\alpha V_{in}, \alpha = \frac{I_{b1}}{I_{b2}} \quad (17)$$

3.1.3. E+ cell

Secondly, the I_A and I_B expressions shown in Fig. 4 are synthesized using two E+ cells. E+ and E- cells were introduced in 1996 as building blocks for the design of log-domain filters (Frey, 1996). They can be built by means of two gate-connected transistors (M1 and M2) as shown in Fig. 7, with M1 being diode-connected. In sub-threshold, the output current of the E+ cell is the exponential of the potential difference between the sources of the transistors:

$$I_{out} = I_0 e^{\frac{V}{nV_t}} \quad (18)$$

Notably, I_0 maps the standard electron transfer constant (k_0) according to equation (11). Additionally, the subthreshold slope (n)

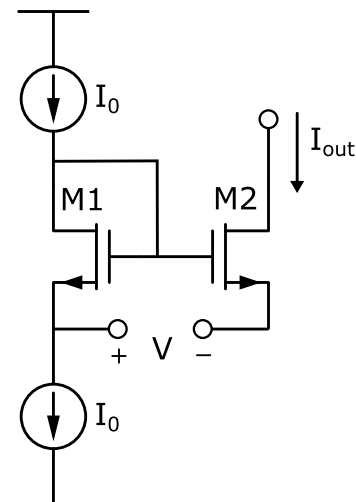


Fig. 7. The E+ cell topology.

appears in the denominator of the exponential term in equation (18), hence, the over-potential (E^*) is scaled by n according to equation (16).

3.1.4. TL multiplier

The expression for I_{IN} is realised by multiplying the output currents of the two E+ cells (I_A and I_B) and dividing by an appropriate unit current (in this case I_0). Fig. 8 illustrates a multiplier circuit that consists of four PMOS transistors of equal aspect ratios, in weak inversion, forming a translinear loop. Through exploiting the translinear principle, the output current is given according to the following equation:

$$I_{out} = \frac{I_A * I_B}{I_0} \quad (19)$$

The output of this block and the output current of the top E+ cell (I_A) are used to generate the currents driving the BC block (i.e. I_U and I_{IN}).

3.1.5. Differentiator

The block in Fig. 9 is used to extract the derivative of the state variable ($\dot{I}_\theta$) embedded in the Bernoulli cell. According to Drakakis et al. (1999) (see Fig. 5), the capacitor current I_{Cap} , the output current I_θ , and its derivative are related by the following relationship:

$$\dot{I}_\theta = I_{Cap} * I_\theta / nCV_T \quad (20)$$

One way to sense the capacitor current is through a two-stage operational amplifier (OpAmp). The virtual ground of the OpAmp ensures that the capacitor is connected to a fixed-value voltage. The output voltage of the OpAmp is then re-converted back into a current proportional to $\dot{I}_\theta$ - and in turn i_F - via the OTAs in Fig. 5, such that:

$$\hat{i}_F \propto I_{Cap} * I_\theta \quad (21)$$

The use of two matched OTAs connected differentially reduces the output offset. Furthermore, the OTAs and the bidirectional current mirrors allow the generation of two copies of the output current in opposite directions. The output currents are connected to the block input ports as shown in Fig. 4.

The block output current ($\hat{i}_F$) is a scaled version of the normalised faradaic current (i_F) according to equation (22):

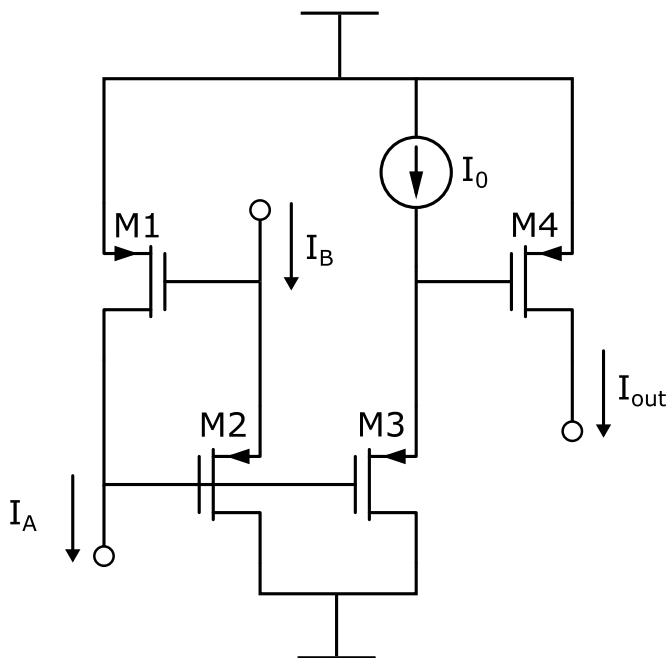


Fig. 8. Type-A PMOS translinear multiplier.

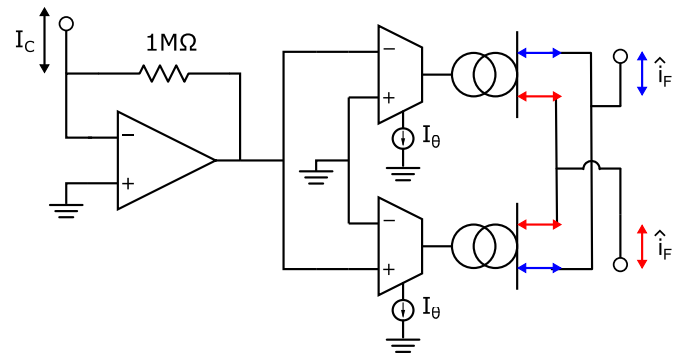


Fig. 9. Topology of the differentiator block which senses the derivative of the state-space variable “hidden” in the Bernoulli cell. The block has two bidirectional ports that are always operating in opposite directions (i.e. if red is sourcing, then blue is sinking and vice versa). For physical realization, the large feedback resistor should be implemented by an active CMOS resistor for noise and size reduction.

$$i_F = S \times \hat{i}_F \quad (22)$$

Where the scaling factor S depends on the transimpedance of the OpAmp, the transconductance of the OTAs, the subthreshold slope factor (n), and the I_Q bias current in the BC block - refer to Fig. 5. Thus, the output current of our element relates to the faradaic current (i_F) via the following equation:

$$I_F = \frac{FAT}{Q} S \times \hat{i}_F \quad (23)$$

This implies that our element models a scaled version of the true faradaic impedance: $\hat{Z}_F$. Hence, in order to preserve the time constants of the reaction, all of the other impedances in the electrical model must be scaled accordingly. For the circuit in Fig. 2, it can be shown that this is achieved by multiplying the resistance by $FAT/S/Q$ and dividing the capacitance by the same factor. The scaling factor (S) can be found empirically from simulations or through calibration of the physical circuit. One approach is to choose a value of S that minimises a certain error function between the circuit output and the ideal mathematical output as will be shown in the Results and Discussion section. Finally, the mapping between the chemical and the electrical parameters is summarised in Table 1.

3.2. Modelling the double-layer capacitance

Several studies have shown it is more accurate to model the double-layer capacitance with a CPE rather than an ideal capacitor (McAdams et al., 1995; Fasmin and Srinivasan, 2017). This is particularly important when the interest is in modelling nonlinear behaviours which is the case for large-amplitude AC voltammetry and nonlinear EIS.

Table 1
Mapping between chemical and electrical parameters.

Chemical Parameter	Electrical Parameter
E^*	$\frac{V_{in}}{n}$
k_0	$\frac{I_0}{nCV_T}$
V_T	$\frac{R_g T}{F}$
θ	$\frac{I_\theta}{I_Q}$
i_F	$\frac{\dot{I}_\theta}{I_Q} \hat{Q}$
α	$\frac{I_{b1}}{I_{b2}}$

The impedance of a CPE is described with the following fractional-order equation:

$$Z(s) = Ds^{-\beta} \quad (24)$$

With $0 < \beta < 1$ for fractional capacitors and $-1 > \beta > 0$ for fractional inductors.

A popular approach (Valsa and Vlach, 2011; Valsa et al., 2011) to emulate CPEs over a broad bandwidth is to use RC networks. We choose to model CPEs as m series blocks, each composed of a resistor and a capacitor connected in parallel as shown in Fig. 10. The impedance is given by:

$$Z(s) = \sum_{k=1}^m \frac{R_k}{1 + sR_kC_k} \quad (25)$$

Where

$$R_k = a^{k-1} * R_1 \quad (26)$$

$$C_k = b^{k-1} * C_1 \quad (27)$$

The recursive scalars a and b are selected depending on the phase angle ripple tolerance ($\Delta\varphi$) and the fractional order (β) according to the following equations (Valsa and Vlach, 2011; Valsa et al., 2011):

$$ab = \frac{0.24}{1 + \Delta\varphi} \quad (28)$$

$$\log(a) = \beta \log(ab) \quad (29)$$

The series resistor (R_s) and the series capacitor (C_s) in Fig. 10 are used to compensate for higher-order terms. They can be derived as the sum of an infinite geometrical sequence of RC blocks (Valsa and Vlach, 2011; Valsa et al., 2011):

$$R_s = R_1 \frac{a^m}{1 - a} \quad (30)$$

$$C_s = C_1 \frac{1 - b}{b} \quad (31)$$

The values of C_1 and R_1 are decided by the designer and the rest of the resistors and capacitors are calculated accordingly. To emulate a CPE with a modulus of D_p , all resistances must be multiplied by the ratio (D_p/D) and all capacitances have to be divided by the same ratio, where D is the modulus of the generated RC network. In our case, we are interested in scaling the charging current I_C similarly to I_F . Hence, we set D_p to the scaled double-layer capacitance ($\hat{C}_{dl}$), which is given by the equation below:

$$\hat{C}_{dl} = \frac{\hat{Q}}{F\Delta F S} \times C_{dl} \quad (32)$$

This method is very simple and can be implemented by connecting commercially available resistors and capacitors externally to the proposed $\hat{Z}_F$ element. However, the resistors and capacitors must be changed to emulate different pseudo-capacitance values. Alternatively, a re-configurable integrated CPE circuit could be synthesized using OTAs connected as active resistors and MOS capacitors with capacitance multipliers.

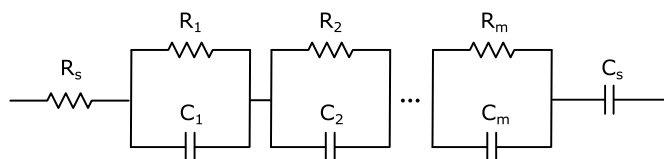


Fig. 10. Schematic of a five-branch RC network model for emulating a CPE. R_s and C_s are corrective elements.

4. Results and Discussion

In this section, the performance of the proposed analogue circuit is evaluated against the ideal BV mathematical model. The circuit has been designed using Cadence Virtuoso and simulated using Spectre in AMS 0.35 μm CMOS process technology. The numerical solution for the BV mathematical model has been programmed using Verilog-AMS. Following the mapping in Table 1, the specific values chosen for the time-invariant electrical parameters, namely the bias currents and the BC capacitor, are reported in Table 2. Notably, the subthreshold slope for the utilized transistors is close to 1; thus the input voltage of the electrical circuit corresponds to the over-potential ($V_{in} = E^*$).

The performance of the analogue model was tested in three ways: Firstly, the $\hat{Z}_F$ element was analysed in transient time and benchmarked against the mathematical model for different AC voltammetry test cases. Secondly, the AC responses of both the $\hat{Z}_F$ and the CPE elements were examined and the functional frequency bandwidth was determined. Finally, the circuit elements were used to emulate an experimental surface-bound Azurin reaction described with the parameters measured by Guo et al. (2004). The circuit model was constructed by connecting the proposed $\hat{Z}_F$ and $\hat{C}_{dl}$ elements in parallel as shown in Fig. 2.

4.1. Transient analysis

The accuracy of the proposed scaled faradaic impedance ($\hat{Z}_F$) element in replicating BV kinetics is examined for AC voltammetry. The current response of the element ($\hat{i}_F$) has been compared against the mathematical model output under different test conditions, where the ideal normalised faradaic current (i_F), produced by the mathematical model, has been scaled by S according to equation (22).

A cyclic input potential, which varies between -80 mV and 80 mV with a scan rate of 160 mV/s, was applied across the two terminals of the $\hat{Z}_F$ element for 4 s. In addition, a 20 mV sinusoidal was superimposed on the cyclic voltage input, similar to the signal in Fig. 1c. The system response has been evaluated for different values of the AC frequency, the standard electron transfer coefficient (k_0) and the electron transfer coefficient (α). The nominal values across the tests are defined in Table 3.

Starting with the nominal values, the frequency was varied between 10 Hz and 100 Hz with 30 Hz step size and including 0 Hz. The response currents of the circuit and the mathematical model are shown in Fig. 11 for the frequency values of 0 Hz, 10 Hz, and 100 Hz. Similarly, the response current was evaluated for k_0 values of 10 s $^{-1}$, 100 s $^{-1}$, 1000 s $^{-1}$ and the results are reported in Fig. 12. Finally, α was set to 0.1 , 0.3 , 0.5 , 0.7 and 0.9 , with Fig. 13 reporting the outputs for the 0.1 and 0.9 test scenarios.

As it becomes evident from the graphs, the response current of the proposed element is almost identical to the ideal response. This is further supported by calculating the normalised root-mean-squared error (NRMSE) between the output of the circuit model $\hat{i}_F$ and the ideal mathematical model scaled (i_F/S):

$$NRMSE = \frac{\sqrt{\frac{1}{T} \int_0^T (\hat{i}_F(t) - i_F(t)/S)^2 dt}}{\max(i_F/S) - \min(i_F/S)} \quad (33)$$

Where T denotes the sampling period. A value for S of 143×10^9 was found to minimise the NRMSE across the above test scenarios. Table 4 summaries the calculated NRMSE results for the presented test scenarios. Overall, the element has excellent accuracy for all test scenarios with a maximum error of less than 3% at very low values of the standard transfer coefficient (k_0). Moreover, the NRMSE value varies little across the different simulations.

Finally, RMS power consumption was calculated for all the above test cases and is reported in Table 4. The average power consumption of the block is 9 μW .

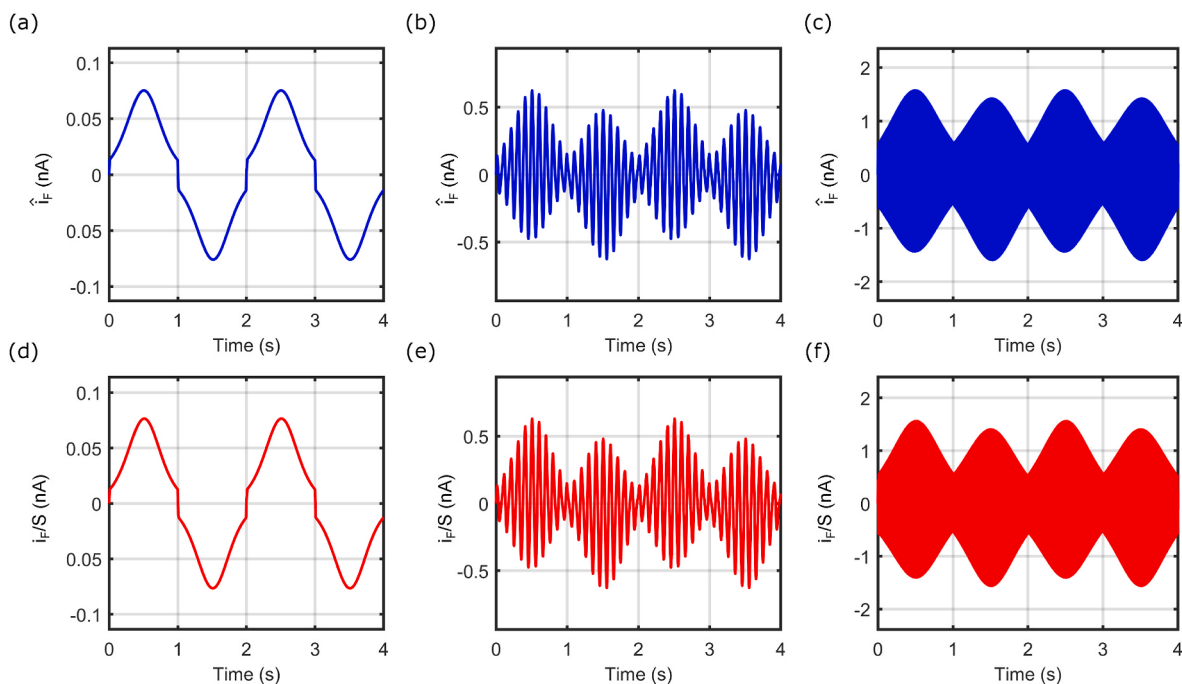


Fig. 11. Comparison of the AC voltammetry response current from the circuit (blue) and the ideal mathematical model (red). The frequency of the sinusoidal input is set to: (a,d) 0 Hz, (b,e) 10 Hz and (c,f) 100 Hz. The rest of the parameters are defined in Table 3.

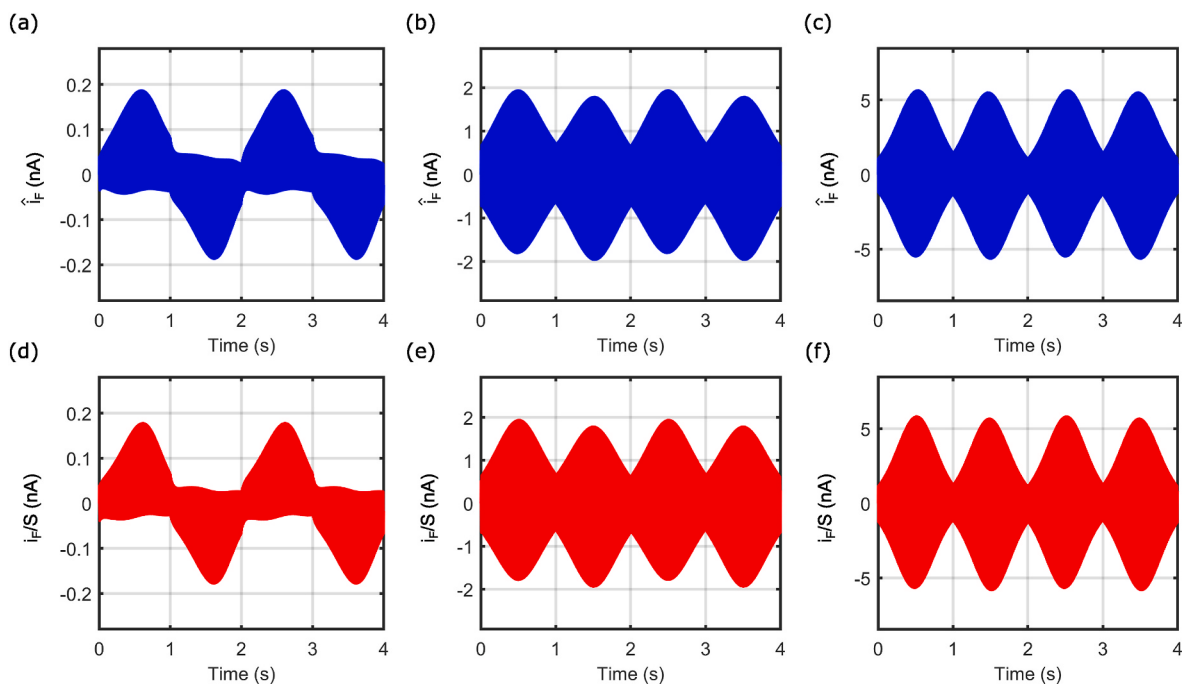


Fig. 12. Comparison of the AC voltammetry response current from the circuit (blue) and the ideal mathematical model (red). The standard electron transfer constant (k_0) is set to: (a,d) 10 s^{-1} , (b,e) 100 s^{-1} and (c,f) 1000 s^{-1} . The rest of the parameters are defined in Table 3.

4.2. AC analysis

Next, the AC response of the proposed $\hat{Z}_F$ element is analysed. Fig. 14 shows the phase and magnitude responses of the circuit and the ideal mathematical model. The responses are identical up to 2 kHz. However, beyond that, the error starts increasing for both the magnitude and the phase due to the impact of parasitics upon the circuit. While further optimisations could be carried out to extend the upper limit of the frequency bandwidth, a bandwidth of 2 kHz satisfies a wide range of

electrochemical processes. Additionally, extending the frequency beyond that would require more circuitry to approximate the $\hat{C}_{dl}$ as will be explained shortly.

As previously mentioned, CPEs accurately model the double-layer capacitance. Detailed treatment of the approach employed to realise CPEs is described by Valsa and Vlach (2011); Valsa et al. (2011). We limit the analysis here to the AC bandwidth of a CPE realised with five RC blocks. Table 5 lists the values of resistors and capacitors necessary to

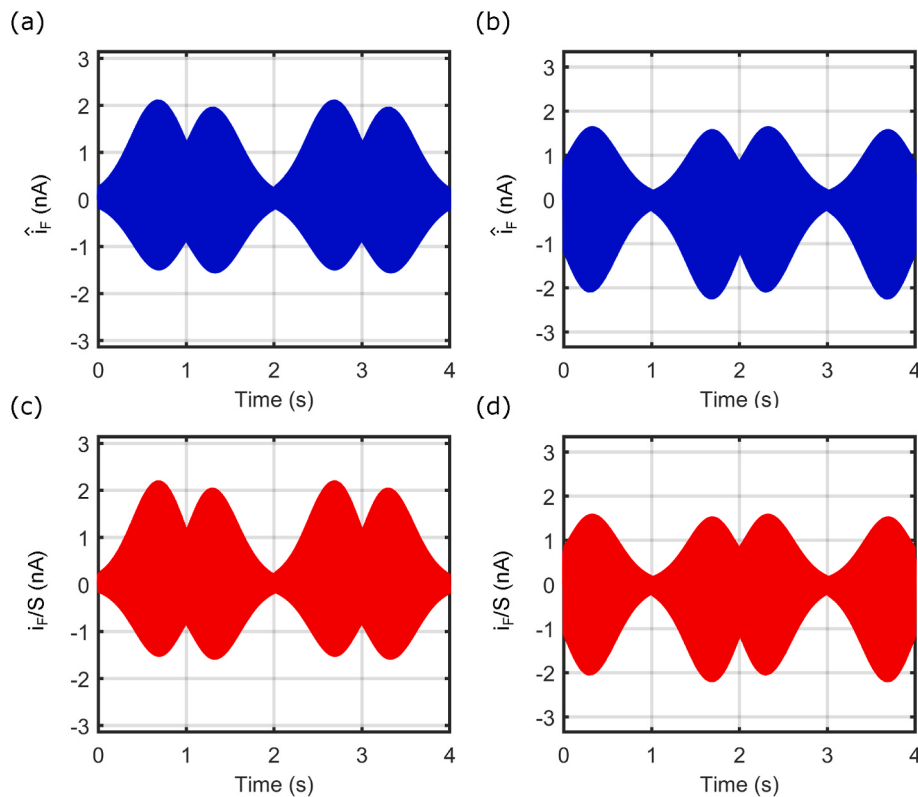


Fig. 13. Comparison of the AC voltammetry response current from the circuit (blue) and the ideal mathematical model (red). The electron transfer coefficient (α) is set to: (a,d) 0.1 and (c,f) 0.9. The rest of the parameters are defined in Table 3.

Table 2
Numerical values for the time-invariant parameters of the BV equivalent circuit.

Variables	Value
C	0.5 nF
I_Q	7 nA
I_{SH}	50 nA
I_{b2}	30 nA
n	1

Table 3
Nominal values of the AC voltammetry test parameters used for the simulations in Figs. 11–13.

Nominal values	
Applied DC potential (E_{dc})	−80 mV–80 mV
Applied AC potential (E_{ac})	20 mV
E_{dc} scan rate	160 mV s ^{−1}
Test scenario # 1	
AC frequency	0, 10, 40, 70, 100 Hz
Standard electron transfer constant (k_0)	80 s ^{−1}
Electron transfer coefficient (α)	0.5
Test scenario # 2	
AC frequency	100 Hz
Standard electron transfer constant (k_0)	5, 80, 100, 1000 s ^{−1}
Electron transfer coefficient (α)	0.5
Test scenario # 3	
AC frequency	100 Hz
Standard electron transfer constant (k_0)	80 s ^{−1}
Electron transfer coefficient (α)	0.1, 0.3, 0.5, 0.7, 0.9

emulate a CPE with a modulus ($\hat{C}_{dl}$) of 10 nF and a fractional order of -0.97 . This fractional-order matches values reported in the literature (Gómez-Aguilar et al., 2016).

Table 4
NRMSE and RMS power consumption values calculated for all tests scenarios given $S = 143 \times 10^9$.

Sweep Parameter	Value	NRMSE (100%)	Power (μW)
Frequency (Hz)	0	0.58	8.89
	10	0.36	8.89
	40	0.56	8.89
	70	0.67	8.89
	100	0.74	8.89
k_0 (s ^{−1})	5	2.95	8.87
	80	0.74	8.89
	100	0.52	8.90
	1000	1.25	9.57
	1000	1.25	9.57
α	0.1	0.75	8.79
	0.3	0.67	8.84
	0.5	0.74	8.89
	0.7	0.84	8.95
	0.9	0.94	9.03

From Fig. 15, the bode plot of the designed CPE shows it has a good AC response in the range between 0.1 Hz and 1 kHz, where the phase error is less than 3°. Using a higher-order RC network with more blocks can further improve the bandwidth; however, such an approach will consume more power. It will also require more components and will occupy a larger footprint.

4.3. Surface-bound Azurin model

Azurin is a well characterized blue copper protein that acts as an electron-transfer agent in the respiratory chain in bacteria (Guo et al., 2004). It is widely used in protein studies (Ortega et al., 2019), biosensor design (Gilardi et al., 1994; Ressine et al., 2010), and the development of emerging bio-optoelectronic devices (Baldacchini et al., 2016). Details on how thin-film Azurin is immobilised on electrode surface can be

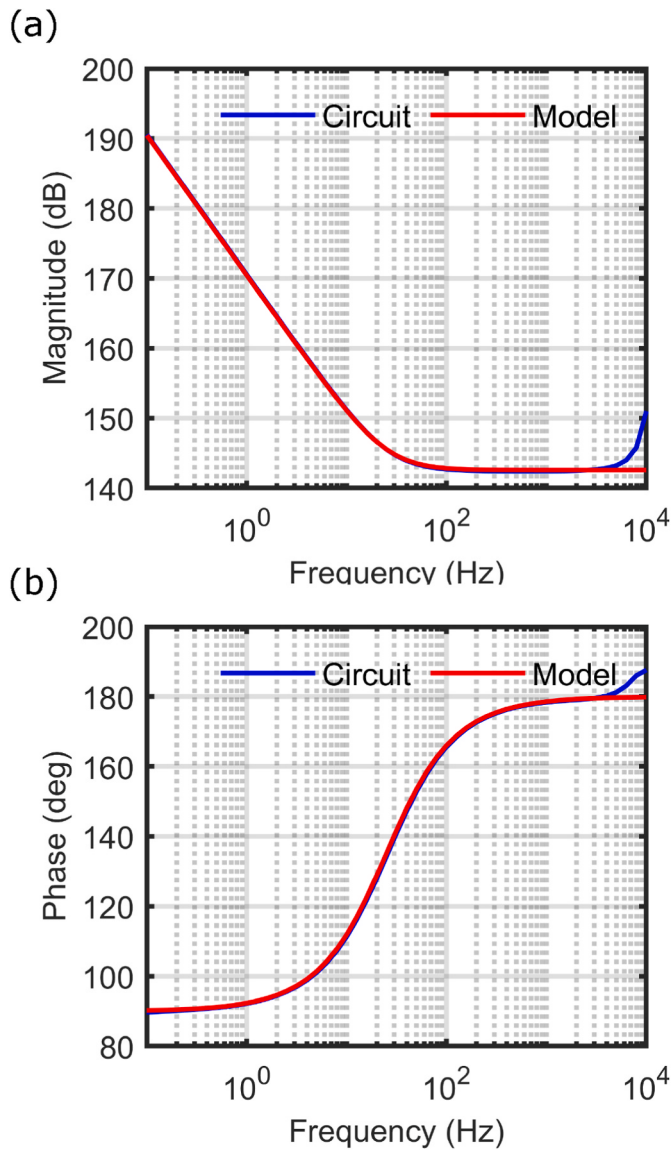
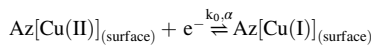


Fig. 14. The Bode plot for the $\hat{Z}_F$ block defined in Table 3.

found in the work of Guo et al. (2004). The Azurin surface-confined redox reaction is given below:



The circuit elements were configured to model the physical surface-bound Azurin reaction with the following reaction parameters: $k_0 = 70 \text{ s}^{-1}$ and $\alpha = 0.5$. These values were calculated from real experimental measurements (Guo et al., 2004). Furthermore, we replicated the exact large-amplitude AC voltammetry setup reported in the same source. Specifically, the E_{dc} potential was swept from +300 mV to −300 mV with a scan rate of 50 mV/s, the AC potential (E_{ac}) was set to 80 mV and the AC frequency was set to 9.54 Hz.

As previously discussed, our circuit produces a scaled version of the ideal faradaic current according to equation (23). Hence, the double-layer capacitance must be divided by the factor $FARs/\hat{Q}$. We choose a CPE impedance of $10 \text{ n s}^{-0.97}$, implemented with the RC components reported in Table 5, to model the scaled double-layer capacitance ($\hat{C}_{dl}$).

The total response current of the circuit is shown in Fig. 16a. From the figure, it can be seen that the charging current dominates the AC voltammogram, which is congruent with the experimental data reported by Guo et al. (2004) and the ideal response in Fig. 17a. This justifies our

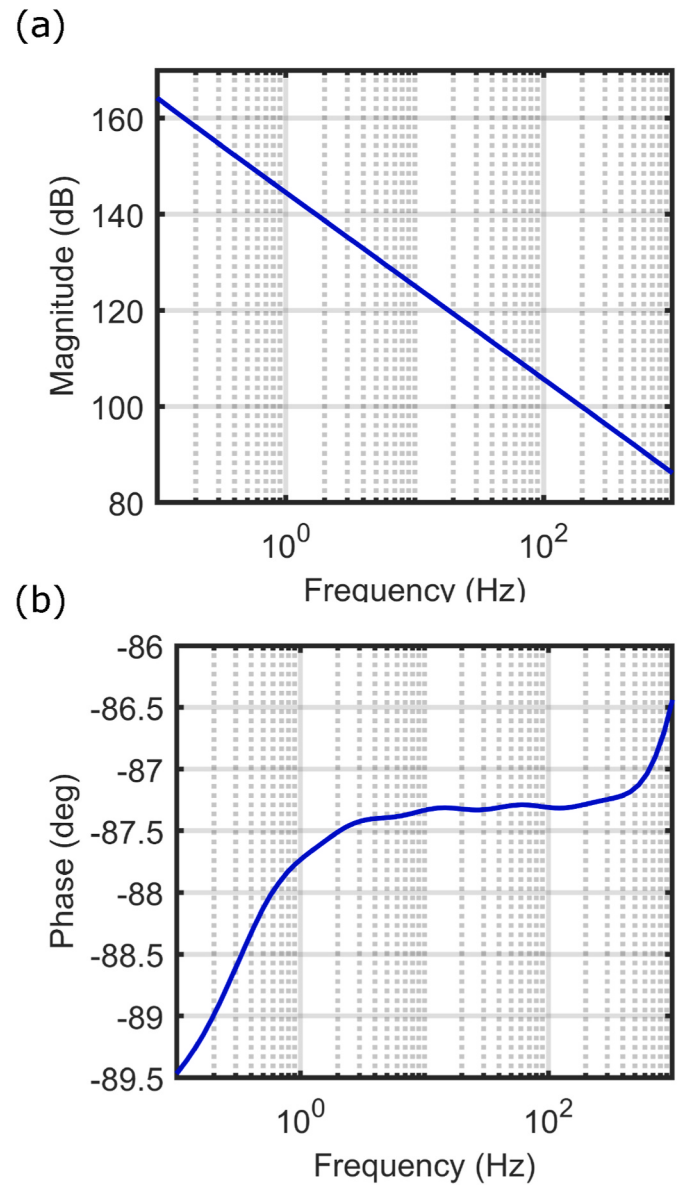


Fig. 15. The Bode plot for the $\hat{C}_{dl}$ block defined in Table 5.

Table 5

RC Network parameter values for the synthesis of a CPE with a modulus of 10 nF and a fractional order of −0.97

Parameter	Value
R_1	1.2 MΩ
R_2	271.4 KΩ
R_3	62 KΩ
R_4	14.2 KΩ
R_5	3.2 KΩ
R_s	957 Ω
C_1	210.34 nF
C_2	200.95 nF
C_3	191.98 nF
C_4	183.41 nF
C_5	175.22 nF
C_s	9.83 nF

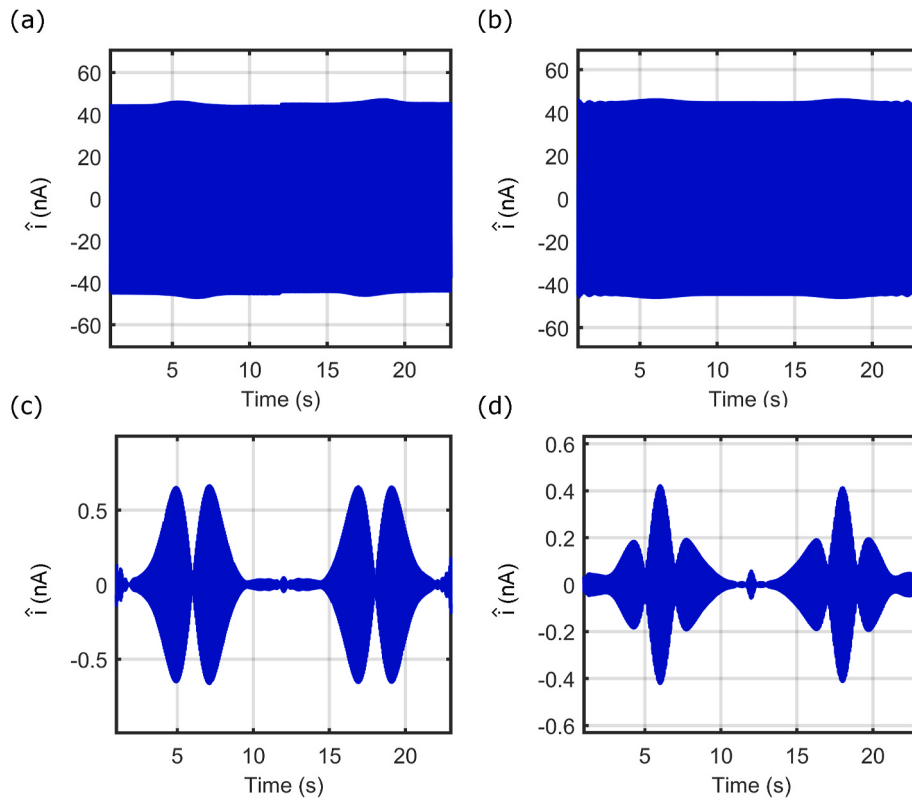


Fig. 16. AC voltammograms of the analog circuit model simulated with frequency = 9.54 Hz, E_{dc} varying from -300 mV to 300 mV, $E_{ac} = 80$ mV, scan rate = 50 mV s^{-1} , $k_0 = 70$ s^{-1} , $\alpha = 0.5$ and $\hat{C}_{dl} = 10$ nF: (a) total current, (b) fundamental component, (c) second harmonic component and (d) third harmonic component.

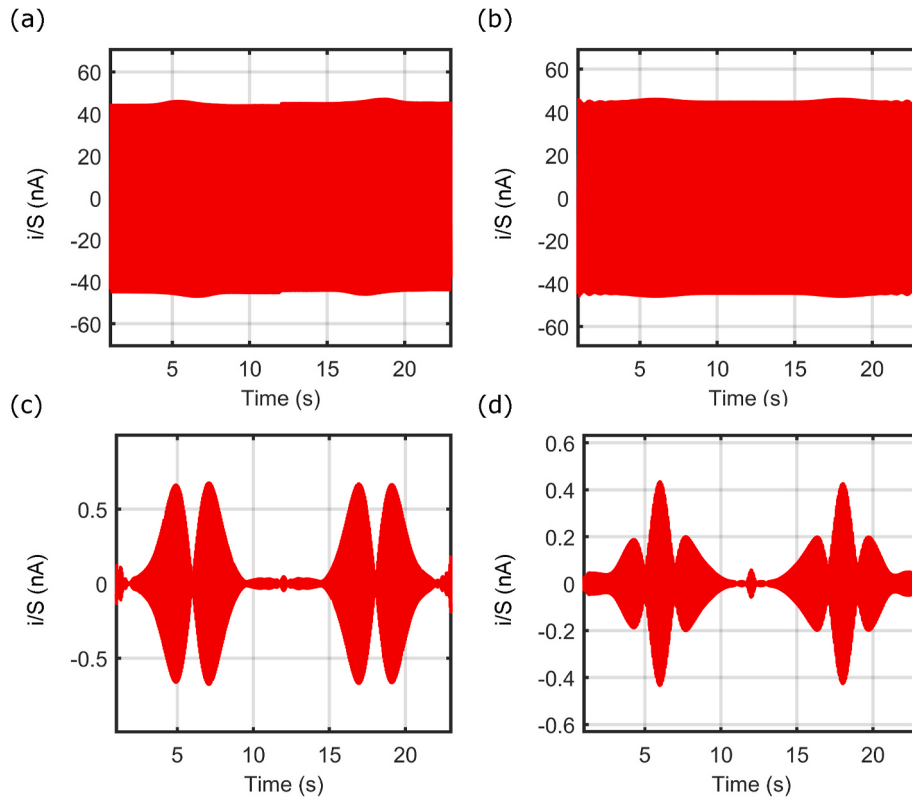


Fig. 17. AC voltammograms of the ideal mathematical model simulated with frequency = 9.54 Hz, E_{dc} varying from -300 mV to 300 mV, $E_{ac} = 80$ mV, scan rate = 50 mV s^{-1} , $k_0 = 70$ s^{-1} , $\alpha = 0.5$ and $\hat{C}_{dl} = 10$ nF: (a) total current, (b) fundamental component, (c) second harmonic component and (d) third harmonic component. $S = 143 \times 10^9$.

value of choice for $\hat{C}_{dl}$.

Finally, the performance is further investigated by plotting the fundamental, second harmonic and third harmonic components of the AC voltammogram as shown in Fig. 16b and c respectively. Qualitatively, the voltammograms match the ones generated using the ideal mathematical model and reported in Fig. 17. The RMS power consumption of the full Azurin model described above is 10.5 μ W.

5. Conclusion

Analogue circuit emulation of electrochemical kinetics is a powerful tool for realising in-situ solvers for reactions differential equations. The circuit could be used with digital peripherals to accelerate the inference of reaction parameters. Potentially, it could also be used for biosensors drift correction by continuously tracking ideal sensor behaviour. This paper presents two elements for emulating the faradaic impedance and the double layer pseudo-capacitance of surface-confined redox reactions. The electrode interface impedance can be modelled by connecting the above-mentioned blocks in parallel and applying appropriate value scaling.

The proposed faradaic impedance element maps the Butler-Volmer chemical variables onto electrical variables in the Bernoulli cell log-domain state-space. The element performance was verified for multiple AC voltammetry test scenarios. The circuit response current was compared with the ideal output of the mathematical model and a maximum NRMSE of less than 3% is reported. Furthermore, the AC response of the proposed element was analysed, and it showed an excellent match up to 2 kHz. Finally, the element consumed an average of 9 μ W.

On the other hand, the double-layer capacitance was modelled as a fractional-order constant phase element (CPE). An RC network was used to approximate the CPE and it was found that five RC blocks are sufficient to match the bandwidth of the proposed $\hat{Z}_F$ element. Finally, both elements were used to emulate a surface-bound Azurin reaction and the results were verified against measured experimental data.

In conclusion, the novel approach and elements proposed in this article accurately emulate surface-confined sensor kinetics for a wide range of test scenarios and can be used as part of a physical solver for reaction parameters. Future work should look into replacing the external resistors and capacitors, required for approximating $\hat{C}_{dl}$, with tunable active elements to produce a fully re-configurable integrated circuit.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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Momen Tageldeen received his B.Eng. in electrical and electronics engineering from Universiti Teknologi PETRONAS (UTP), Malaysia, in 2015. He received an M.Res. in Bioengineering from Imperial College London, UK, in 2016, with a focus on software/hardware co-design for wearable and wireless electronics for electrochemical traumatic brain injury monitoring. In 2022, Dr. Tageldeen received his PhD from Imperial College London under the supervision of Prof. Emmanuel Drakakis. His research centred on electronics design for ultrasound imaging and AI compute acceleration.

Dr. Tageldeen is currently a senior ASIC designer with AMD, where his work focuses on the design of video cores and digital hardware accelerators.



Ilias Pagkalos received the Dipl.Ing. degree in electrical and computer engineering from Democritus University of Thrace, Xanthi, Greece, and the M.Sc. degree in analogue and digital integrated circuit design from the Department of Electrical and Electronic Engineering of Imperial College London (ICL), London, U.K., in 2011 and 2012, respectively. In 2016, he received his Ph.D. from the Department of Bioengineering at ICL under the supervision of Prof. Emmanuel Drakakis. His research interest focused on Traumatic Brain Injury (TBI) and the design and testing of a high-performance application specific integrated circuit for electrical and neurochemical TBI monitoring.

Currently he is a senior data scientist with Capgemini focusing on the utilisation of data and machine learning to create value-added solutions to business problems.



Sara Ghoreishizadeh is a lecturer in Bioelectronics at Dept of Electrical and Electronic Eng., University College London (UCL), UK, where she leads an interdisciplinary research team on analogue/mixed-signal Integrated Circuit (IC) design and CMOS biosensors for new applications in point-of-care and wearable technologies for real-time quantitative analysis of health conditions such as physiological stress, oral health and acute pain.

Dr Ghoreishizadeh received a PhD from Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland, in 2015 and has been with Imperial College as a Postdoctoral Research Fellow during 2015–2018. She is a fellow of the Higher Education Academy (FHEA) and a member of IEEE, and IEEE CAS, SSC and EMB societies. She is an associate editor of IEEE TBioCAS and has been elected to the IEEE CAS Board of Governors (BoG) for the period of 2020–2022.



Emmanuel M. Drakakis (M'05) received the 4-year B.S. degree in Physics and the 2-year M.Phil. degree in Electronic Physics and Radioelectrology from Aristotle University of Thessaloniki, Macedonia, Greece, and the Ph.D. degree in IC design from Imperial College, London, U.K. Currently, he is Professor in Bio-Circuits and Systems with the Department of Bioengineering, Imperial College London where he also serves as Deputy Head. In this Department, he has founded the Bio-inspired VLSI Circuits and Systems Group, whose research focuses on “Circuits for and from Biology and Medicine”. He has authored or co-authored a large number of peer-reviewed papers and several book chapters. He is the recipient of many prizes for research excellence and is involved in numerous cross-disciplinary, multi-million research projects. He is currently Associate Editor with *Frontiers in Neuromorphic Engineering* and an Editorial Advisor with *BMC Biomedical Engineering*, Springer Nature. In the past he has served as Editor with *Measurement-Elsevier*, Associate Editor with *IEEE Transactions* (IEEE TBIOCAS, IEEE TCASI and IEEE TCAS-II) for a total of nineteen years, Subject Editor with *International Journal of Electronics* and Guest Editor with *IEEE ELettters*. He has a cumulative editorial service to the research community of thirty-five years.