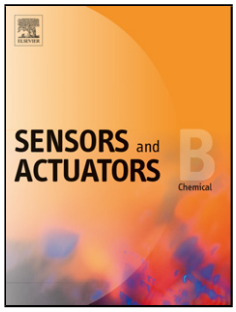

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PII: S0925-4005(18)31767-2
DOI: https://doi.org/10.1016/j.snb.2018.10.004
Reference: SNB 25437

To appear in: *Sensors and Actuators B*

Received date: 3-5-2018
Revised date: 16-9-2018
Accepted date: 1-10-2018

Please cite this article as: Dudina A, Seichepine F, Chen Y, Stettler A, Hierlemann A, Frey U, Monolithic CMOS sensor platform featuring an array of 9'216 carbon-nanotube-sensor elements and low-noise, wide-bandwidth and wide-dynamic-range readout circuitry, *Sensors and amp; Actuators: B. Chemical* (2018), https://doi.org/10.1016/j.snb.2018.10.004

Monolithic CMOS sensor platform featuring an array of 9'216 carbon-nanotube-sensor elements and low-noise, wide-bandwidth and wide-dynamic-range readout circuitry

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Abstract

We present the design and characterization of a monolithic complementary metal–oxide–semiconductor (CMOS) biosensor platform comprising of a switch-matrix-based array of 9'216 carbon nanotube field-effect transistors (CNTFETs) and associated readout circuitry. The switch-matrix allows for flexible selection and simultaneous routing of 96 sensor elements to the corresponding readout channels. A low-noise, wide-bandwidth, wide-dynamic-range transimpedance continuous-time amplifier architecture has been implemented to facilitate resistance measurements in the range between 50 kΩ and 1 GΩ at a bandwidth of up to 1 MHz. The achieved accuracy of the resistance measurements over the whole range is 4 %. The system has been successfully fabricated and tested and shows a noise performance equal to 2.14 pA_{rms} at a bandwidth of 1 kHz and 0.84 nA_{rms} at a bandwidth of 1 MHz. A batch integration of the CNTFETs has been achieved by using a dielectrophoresis (DEP)–based manipulation technique. The current-voltage curves of CNTFETs have been acquired, and the sensing capabilities of the system have been demonstrated by recording resistance changes of CNTFETs upon exposure to solutions with different pH values and different concentrations of NaCl. The smallest resolvable concentrations for the respective analytes were estimated to amount to 0.025 pH-units and 4mM NaCl.

Keywords

Carbon nanotube field-effect transistor, CMOS, ion-sensitive field-effect transistors, chemFET

Introduction

Since the first electronic transport measurements were performed on individual carbon nanotubes (CNTs), tremendous progress has been made in understanding their electronic structure and their electronic transport properties [1]. Based on these findings, a number of applications for nanotubes has been proposed ranging from microelectronic components like interconnects to field-effect-transistor (FET)-based sensor structures for use in gaseous or liquid phase [2], [3].
Owing to their unique geometric and electronic properties, CNTs offer great potential for chemo- and biosensor applications. Their small size and high surface-to-volume ratio makes CNTs extremely sensitive to the changes in the gaseous or liquid chemical environment. It has been shown that functionalized, liquid-gated CNTFETs are capable of detecting analytes in the picomolar range [4]. High-bandwidth properties of CNTs make them a promising transducer to observe fast dynamics at single-molecule resolution [5,6].
The CNTFET sensing mechanism is similar to that of ion-sensitive FETs, namely the chemical solution or charged molecules influence the gate region. The presence of a charged analyte in close proximity to the CNTFET, modulates the CNT conductance and, consequently, the drain-source current flowing through the FET [7]. In Figure 1 a general representation of a CNT device, configured as a liquid-gate FET (LG-CNTFET), is shown.

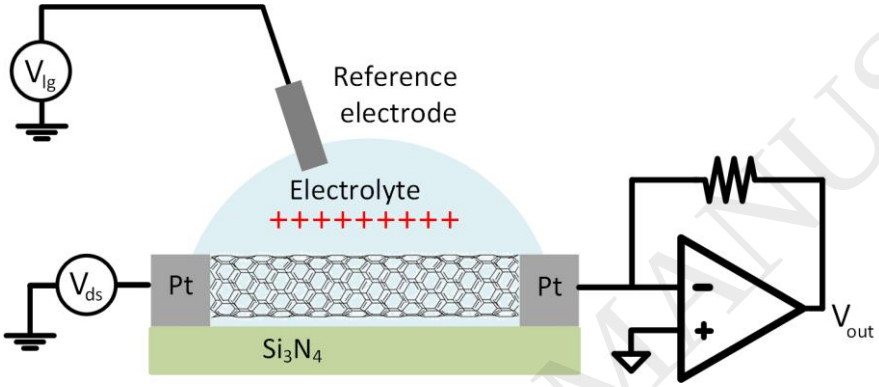

Figure 1: Sensor configured as a liquid-gate CNTFET (LG-CNTFET). The device is gated through the electrolyte by V_{gs} (gate-source voltage). V_{ds} (drain-source voltage) defines the conductance of the LG-CNTFET. I_{ds} is the drain-source current. V_{out} is the measured voltage that corresponds to the measured current, converted to a voltage by means of a resistive-feedback gain stage.

However, the inherently large variation in the CNT physical properties, such as the nature of the CNTs (metallic or semiconducting, single or multiwall), the spread in the CNT baseline conductance, the variation of geometrical parameters, limits the use of CNTs in bio-sensing devices for point-of-care diagnosis or label-free sensing.
The integration of large numbers of CNTFETs into sensor array platforms will help to overcome some of these issues by providing redundancy in CNT sensors and the possibility to extract average values. Moreover, the parallel measurements of many sensor elements can be done under conditions of approximately constant temperature or electromagnetic interference and while non-specific sensor responses remain essentially identical. This is an important aspect for conducting quantitative measurements of biological parameters, as large numbers of sensors allow for obtaining statistically significant data even in noisy environments. Furthermore, arrays of differently functionalized sensors can be realized on the same platform and allow for multiplex sensing.

An important aspect of integrated CNT sensor systems is the careful design of the readout and amplification circuitry. Typically, the conductance change, induced by a change in analyte concentration, or by the presence of a single molecule, depends on the initial baseline conductance of the CNT device. For single-molecule sensing applications, the conductance changes can be in the range of hundreds of nS, and the required measurement bandwidth can be up to few hundreds of kHz [8], so that appropriate low-noise, wide-bandwidth integrated circuits are needed to read out such minute changes. The signals have to be amplified so that they can be processed afterwards. Moreover, the readout circuits

need to cope with a large spread in the CNTFET baseline conductance, which can vary by two orders of magnitude. A good compromise for the performance of the circuits with respect to functionality and targeted signal quality needs to be found.
Due to connectivity issues, the parallel readout with external low-noise amplifiers is not feasible, in particular, as the bandwidth performance of such a hybrid system will be limited by the large parasitic resistances and capacitances of the interconnects.
The use of CMOS technology helps to overcome most of the issues described above. The realization of a monolithic sensor platform featuring CNTFETs integrated with CMOS technology enables a flexible selection and parallel readout of many sensors in parallel. Moreover, the sensors and the readout circuits can be positioned in close proximity to each other so that the signal-to-noise ratio (SNR) can be improved. Additionally, the parasitic capacitances are reduced and the measurements can be performed with higher bandwidth.
Extensive work has been done in the field of CMOS readout circuits for CNT sensors [9–12]. Some work has been published on the design and fabrication of monolithic systems that feature sensor arrays and readout circuitry on a single chip [13–16]. Most of the papers feature only a few readout channels or smaller arrays of sensors , e.g., less than 100 sensors, as reported in [10,14,17].
Typical architectures for current readout circuits are based on either current-to-time (C-T) conversion or current-to-voltage (C-V) conversion methods. In C-T conversion, the change in the measured current is converted into a digital pulse stream, typically by using a sigma-delta readout architecture. With this approach no additional ADC is required, as the sensor signal is measured and digitized at the same time [18]. Additionally, the power consumption of the corresponding readout architecture is relatively low. The disadvantage of the sigma-delta approach is the limited bandwidth between few tens of Hz up to few tens of kHz. Therefore, a sigma delta architecture is only suitable for slowly varying signals. For some applications, however it is beneficial to have a measurement bandwidth of up to 1 MHz [8]. An alternative method is to convert the measured current to a voltage via a variable trans-resistance gain. The advantages of the corresponding circuitry include a flexible bandwidth, a wide dynamic input range, and low-noise performance, however at the expenses of increased circuit real estate and power consumption. In particular for the CNT-based sensor arrays, the trans-resistance approach is beneficial, as it can deal with a large variation in sensor resistances by means of a variable resistance gain without a loss in the measurement bandwidth. However, an additional ADC is required to convert the voltage signal into a digital code [13].

Another issue in designing sensor arrays arises from multiplexing and the resulting leakage currents. This issue can be avoided by implementation of arrays with dedicated readout channels [15]. The major challenges in designing large-scale CNT sensor arrays include the trade-offs between overall size of the array, the limited area for the circuits within each pixel, the overall number of sensors, and the flexibility in routing sensors to readout channels.
In this paper we propose a sensor array, which is based on the switch-matrix approach [19], where a subset of sensors can be selected and connected to readout channels. The use of a switch-matrix-based routing in the array helps to achieve flexibility in sensor selection and a parallel readout of a large number of sensors, while at the same time preserving good signal-to-noise characteristics. Additionally, a higher density of sensors in the array can be achieved, as the routing is realized by means of CMOS switches, which are located underneath the sensors in the array. Moreover, the inactive sensors can be disconnected from the readout paths so that leakage currents and parasitics are reduced.

The system described here includes an array of 96x96 sensor elements and 96 dedicated readout channels. The readout channels are implemented as trans-resistance amplifiers with tunable gain and bandwidth settings. The whole array can be quickly scanned in a block–wise fashion to measure the conductance values of all the CNT sensors. Subsequently, a subset of up to 96 sensors can be read out in parallel at low noise and high bandwidth. To

the best of our knowledge, this is the largest CNT-based monolithic sensor array with integrated readout amplifiers implemented in CMOS technology.

System description

A schematic of the overall system is shown in Figure 2. Each block will be described in more detail in the following sections.

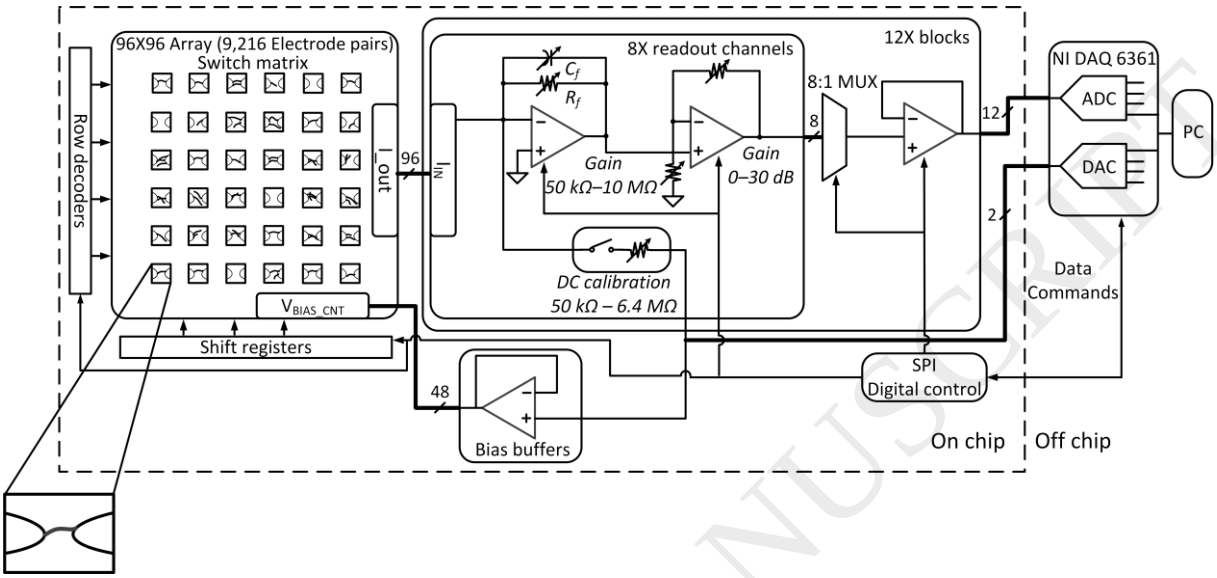

Figure 2: Block diagram of the developed system.

CMOS chip

Array

The array has 9,216 pixels and has a size of 2.16×1.44 mm^2. Each pixel consists of a pair of platinum electrodes. Each electrode pair provides the source and the drain connection for a CNT-FET. One source electrode is shared between two adjacent drain electrodes. The underlying electrode routing is switch-matrix based, similar to [20]. The architecture of a pixel is shown in Figure 3 (a).

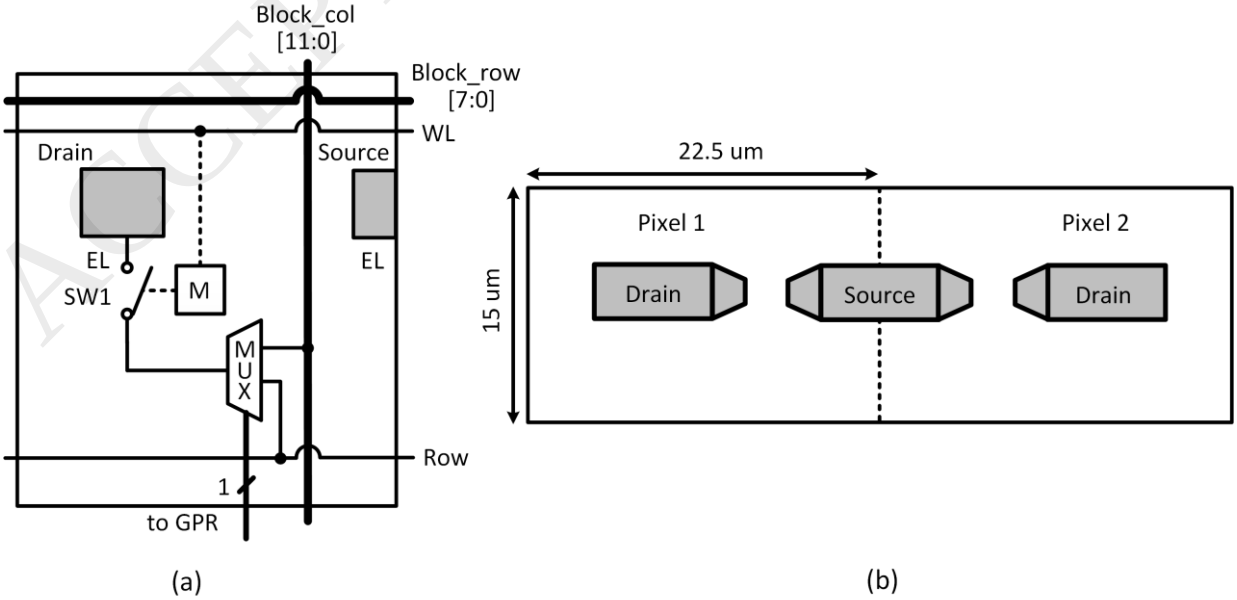

Figure 3: (a) Block diagram of the architecture of one pixel where M is a 1-bit memory cell and EL represent the connection to the Drain and Source electrodes. (b) Layout sketch of two adjacent pixels with three electrodes (EL). The size of the full array is 2.16x1.44 mm^2.

Each array pixel contains one SRAM memory cell (M), a switch (SW1) and a 1:2 multiplexer (MUX). M controls the state of the switch SW1, which connects the electrode to the MUX. The configuration of the array in row or block mode is done by enabling one of MUX outputs, which routes the corresponding electrode to the readout channel. MUX comprises of two switches and is controlled by one bit of a global general-purpose register (GPR). A parallel readout of 96 elements located in one column, or in a 12×8 block in any region inside the array is possible[20]. The routing for the shared source electrode is implemented in a similar manner. The array is programmed via a serial peripheral interface (SPI), clocked at 20 MHz. General-purpose registers (GPRs) are used to store digital settings for the chip amplifiers and can be accessed via the SPI according to their unique physical address. The programming procedure for one 8-bit GPR takes two SPI commands for setting the address and writing the value. A burst mode allows for programming consecutive GPRs with incrementing the address automatically.
The sketch of two adjacent pixels is shown in Figure 3 (b). Due to the small size of 22.5×15 µm^2 of one pixel, the realization of a large-scale array with many sensors at high density is possible. Here, a density of 2'963 CNTFETs/mm^2 was achieved. The size of the platinum electrode is 6.5x3.5 µm^2, and the capacitance, C_{el}, is estimated to 18 pF. Based on simulations of the extracted pixel circuit, the contribution of the parasitic capacitance of the wiring in the switch matrix, C_{sm}, is - in the worst case - 5 pF, and the resistance of all three switches between electrode and readout channels, R_{sm}, is approximately 7 kOhm. The parasitic capacitance and resistance generate a low-pass filter for the measurement signal as shown in Figure 4.

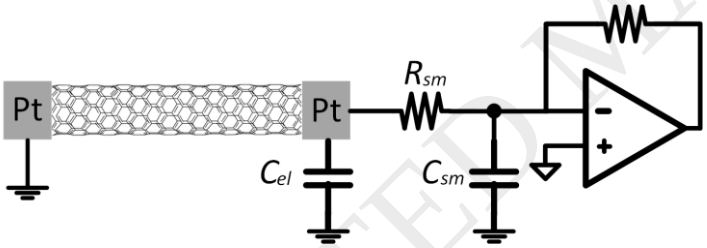

Figure 4: Contribution of parasitics to the measurement bandwidth. C_{el} is the electrode capacitance, R_{sm} – parasitic resistance of the switch-matrix interconnects, C_{sm} – parasitic capacitance of switch-matrix interconnects. Pt – platinum electrodes.

The measurement bandwidth can be calculated as the 3dB bandwidth of an RC circuit. In this particular design, the measurement bandwidth is approximately 1 MHz. However, it has been shown that the intrinsic bandwidth of the CNT device can be as large as 10 MHz [13].

Readout channels

The chip has 96 readout channels, each of them including two stages of amplification and filtering, followed by a multiplexer (MUX) and a driving buffer, see Figure 5.

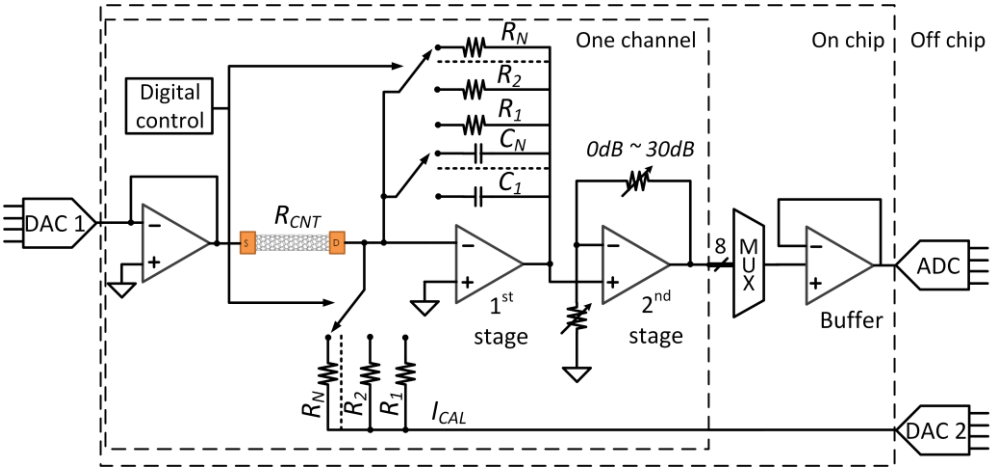

Figure 5: Block diagram of the readout channel. $R_{1\text{-}N}$, denote variable resistive feedback gain and resistive calibration ladder; $C_{1\text{-}N}$ denote feedback capacitors for tuning the bandwidth of the first-stage amplifier. DAC, ADC are digital-to-analog and analog-to-digital converters respectively.

In order to meet the requirements of low noise and a tunable bandwidth, a continuous-time trans-impedance-amplifier (TIA) architecture has been chosen. The amplifier gain is programmable with a 6dB step value, so that the amplifier can handle currents ranging from tens of picoAmperes to microAmperes. The amplifier bandwidth is also tunable, which enables to maximize the front-end bandwidth while maintaining amplifier stability. The core operational transconductance amplifier (OTA) for the TIA is realized by a two-stage Miller-compensated, rail-to-rail-input and rail-to-rail-output amplifier, see Figure 6.

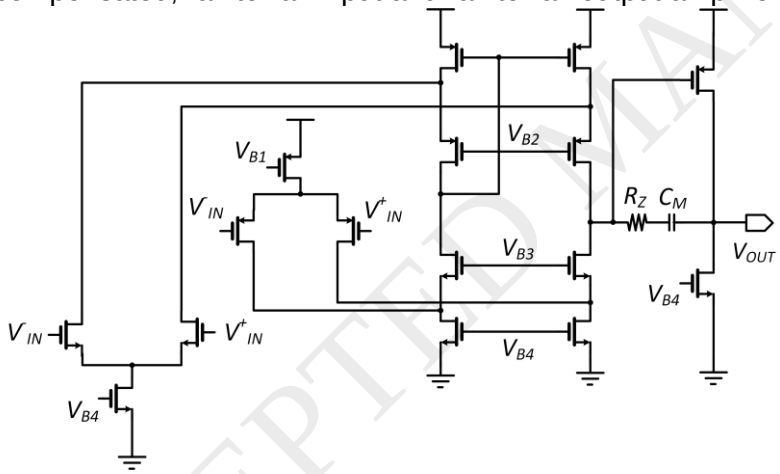

Figure 6: Architecture of the core operational transconductance amplifier (OTA) for the transimpedance amplifier (TIA).

A rail-to-rail input stage architecture has been chosen to allow for flexibility in the common-mode voltage. The possibility of sweeping the common-mode voltage is important for obtaining the characteristics of the CNTFETs, such as the I-V curves, where the sweeping of the voltage over several Volts is required. The second gain stage is needed to achieve a high total loop gain and to retain a high swing at the output. The design of the OTA for the TIA stage has been optimized in terms of noise performance, power consumption and stability over a wide range of feedback resistances and capacitances.

The second stage is a variable-gain amplifier. It provides additional gain (from 0 to 30 dB at 6 dB steps) and limits the bandwidth to prevent aliasing. The output of every channel is multiplexed to the output buffers, and, finally, the data are digitized by 16-bit external analog-to-digital converter (ADC, National Instruments data acquisition card (DAQ) 6361). The multiplexer is controlled externally with the help of the DAQ card. All 96 channels can be

read out simultaneously at a measurement bandwidth of up to 30 kHz per channel, or a smaller subset of sensors can be read out at higher frequencies of up to 1 MHz.

Each channel has a dedicated digital block, which allows for independent gain and bandwidth selection. In order to compensate for the offset and gain error, a resistive feedback loop has been implemented in each channel. An offset voltage can add errors to the measurement of the baseline conductance of the sensor, as the bias voltage of the CNT is not precisely defined. The offset compensation can be done by using six different resistor values, in a similar way as reported by Grassi et al. [9].
The chip includes 48 voltage buffers to define the voltages at the source terminals of each CNTFET. Each voltage buffer is an operational amplifier, configured in unity-gain feedback, which provides voltages in the range from 200 mV to up to 3.2 V. It can drive a capacitive load of up to 1 nF and a minimal restive load of 10 kOhm.

Fabrication

The CMOS chip has been fabricated in 0.18-µm-CMOS technology, and the overall chip real estate was 6.4x3.0 mm^2. Pairs of platinum electrodes were patterned at wafer level by means of ion-beam metal deposition and etching. A multilayer SiO_2/Si_3N_4 passivation stack was deposited by plasma-enhanced chemical vapor deposition (PECVD) to protect the CMOS circuits against the saline solution. Finally, the electrode area and wire bonding contacts were opened by a reactive-ion-etching (RIE) step. An SEM picture of Pt electrodes is shown in Figure 7.

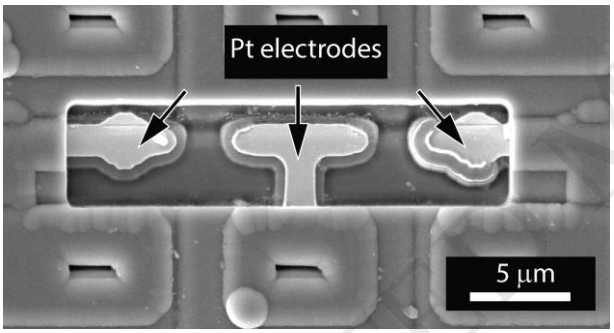

Figure 7: *Surface of the CMOS chip after the fabrication process. Platinum electrodes are visible in the opening in the SiO_2/Si_3N_4 passivation layer.*

Measurement Setup

The CMOS chip was wire bonded on a custom-designed printed circuit board (PCB). A microfluidic system has been developed to deliver the liquid solution to the sensing area and to protect the interface electronics. A simple microfluidic chamber, fabricated from a preformed poly(dimethylsiloxane) sheet (PDMS) was placed on top of the sensor array. The chamber was clamped between two poly(ethyleneterephtalate) supports (PET), and holes for inlet and outlet tubes as well as for the Ag/AgCl reference electrode were punched. The solution was pumped into the chamber by a syringe pump. The volume of the chamber was approximately 10 µl. The PCB has been mounted on custom-designed setup board which provides analog power supply and reference voltages. In Figure 1Figure 8 (a) the final system is presented. In Figure 8 (b) the detailed schematic is shown.
Data processing and communication was done through the DAQ card. A dedicated LabVIEW (National Instruments) based graphical user interface has been implemented to communicate with the CMOS chip. The recorded data sets have been analyzed in MATLAB (Mathworks).

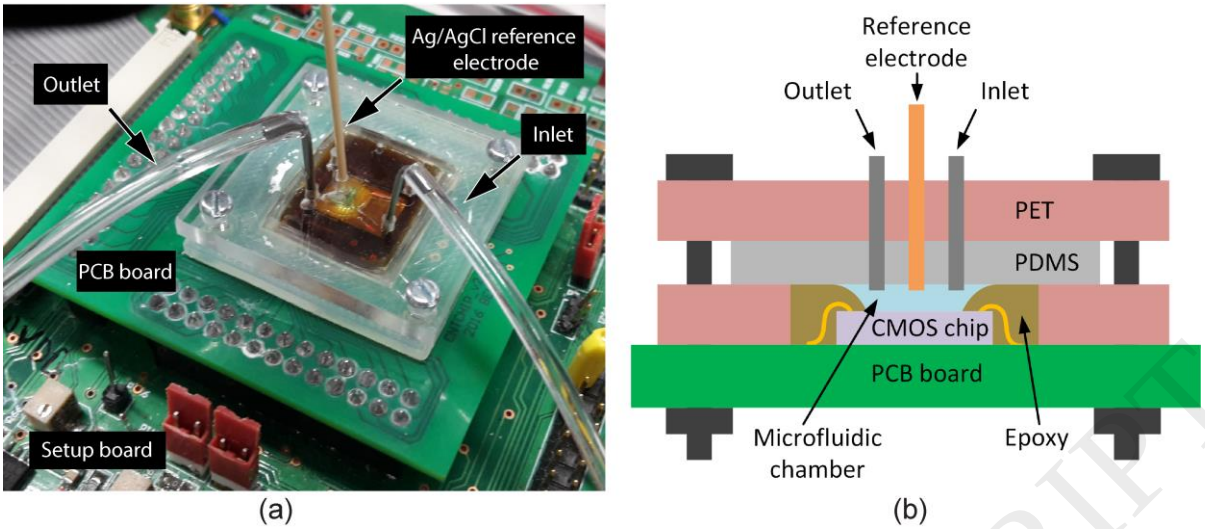

Figure 8: (a) Packaged system mounted onto the setup board for experiments with liquid solutions. (b) Schematic cross-section of the packaged system.

Electrical characterization

The electrical characterization of the chip has been carried out to assess gain and noise performance. Figure 9 (a) shows the gain characterization measurements. For these measurements, the gain of the second stage was set to 30 dB, and the feedback capacitor of the first stage was set to 10pF. The gains ranged from 105 dBOhm, which is equivalent to 50 kOhm, up to 140 dBOhm, which is equivalent to 9.7 MOhm, resistive feedback gain. Figure 9 (b) shows the variation of the 1 MOhm resistive feedback gain across all 96 channels of one chip. The measured gain has a good uniformity with a σ of 40.4 kOhm.

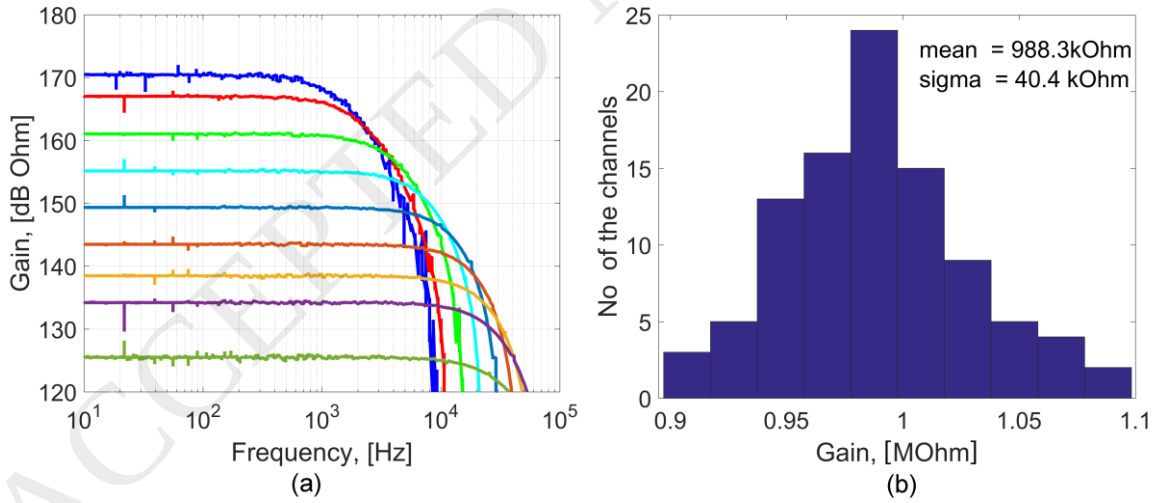

Figure 9: (a) Gain curves over the entire available frequency range. (b) Variation of the 1-MOhm resistive feedback gain over 96 channels.

In Figure 10 (a), the input-referred power spectral density (PSD) of the current noise of the readout channels has been plotted for a gain of 200 kOhm and a bandwidth of 1 MHz. The PSD in the plot have been averaged over 10 channels. The feedback capacitance for the noise measurements was set to 9 pF, and the gain of the 2nd stage was set to 0 dB. The array was immersed in phosphate-buffered saline solution (PBS) and a potential of 0 V was applied through the reference electrode (V_{LG}). For the reference electrode, a low-noise Yokogawa voltage source was used. The noise of the readout channel was measured with

the first stage connected to a platinum electrode in the array. The area of the electrode was 6.5 x 3.5 μm^2, and the capacitance, Cel, was estimated to be 18 pF. The impedance of the electrode was calculated to be approximately 5 GOhm at a frequency of 1Hz. In Figure 10 (b) the integrated current noise is shown within a frequency range of up to 1 MHz.

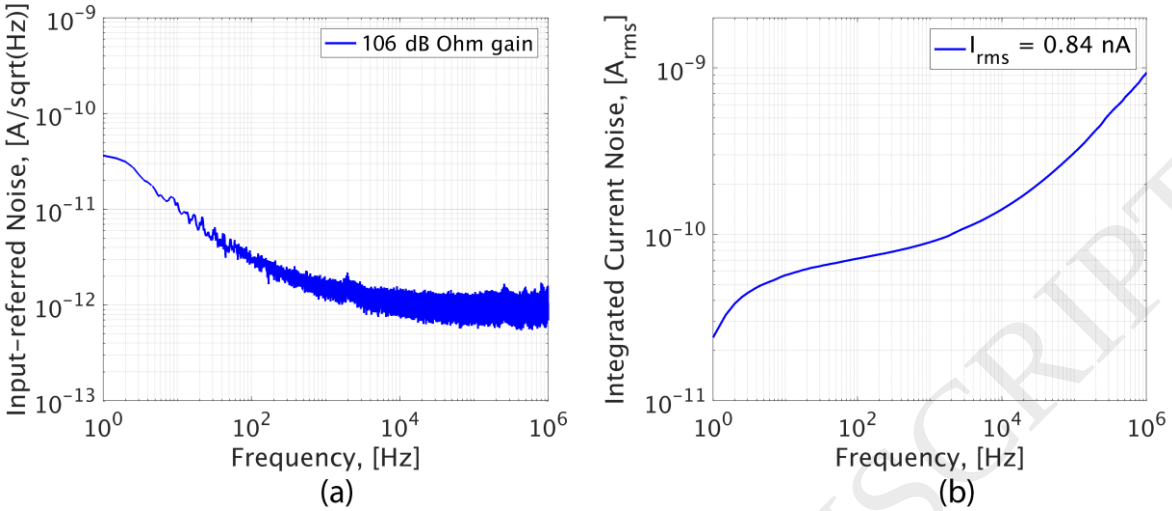

Figure 10: (a) Input-referred current noise PSD of the readout channel with 200 kOhm feedback gain; (b) current noise integrated over the displayed frequency range up to 1 MHz.

Table 1 one gives an overview of the designed system and compares the obtained results with state-of-the-art work.

Table 1: Comparison with state-of-the-art work.

Parameter	Livi et al., 2015 [17]	Cho et al., 2009 [12]	Shin et al., 2013 [10]	This work
Technology	0.35 μm	0.13 μm	0.18 μm	0.18 μm
Chip area	3.4×4 mm^2	0.173 mm^2	1.0×0.7 mm^2	6.4×3.0 mm^2
Sensor array	On chip	Off chip	Off chip	On chip
No. of sensor elements	16	24	64	9,216
Input Range	7 kΩ - 7.5 GΩ	15 kΩ – 1.5 MΩ	10 kΩ – 9 MΩ	50 kΩ – 1 GΩ
No. of channels	16	64	24	96
Bandwidth	~1 kHz	~1 kHz	1.83 kHz	~1 MHz
Noise (input-referred) over 1 Hz – 1kHz	0.54/250 pArms	2 pArms	2.5 pArms	2.14 pArms
Power supply	3.3 V	1 V	1.2 V	3.3 V

CNTFET assembly and characterization

The CNTs were assembled on the chip by means of a dielectrophoresis (DEP)-based deposition technique [16]. Dielectrophoresis describes the motion of particles, suspended in a solvent, as a consequence of applying an inhomogeneous electrical field [21]. The principle is illustrated in Figure 11.

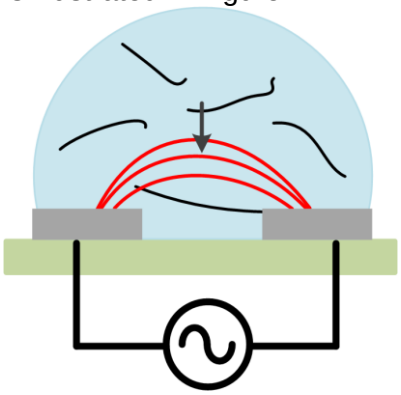

Figure 11: DEP-based assembly. A droplet of a suspension containing CNT devices is placed on the electrode surface. The electrodes are connected to an AC generator, which produces an electrical field between the electrode pairs and generates DEP forces to manipulate the CNTs in suspension.

A big advantage of DEP assembly process is its compatibility with the CMOS technology, as it is usually performed at room temperature. Moreover, through the use of specific electrode geometries and control of deposition parameters, DEP can be used to assemble devices ranging from single, individual CNTs to high-density carpets of CNTs with controlled orientation [22].
The electric field between the electrodes, which was required for DEP deposition, was generated by configuring the switch-matrix to connect the respective electrode sets. The approach is illustrated in the **Error! Reference source not found.**Figure 12 (a) and Figure 12 (b). The selected electrode sets were connected to two pads of the CMOS chip, (Figure 12 (b)) by configuring the multiplexers (MUX) and corresponding switches underneath the electrodes.
The CNT suspension preparation has been adapted from [16]. CNTs, single-walled and carboxylic-acid functionalized were purchased from Sigma Aldrich, Buchs, Switzerland. A powder of CNTs was dispersed in de-ionized water at a concentration of approximately 80 µg/L. A sonication of the solution of 30 min and a centrifugation at 150,000 rpm for 30 min enabled to obtain a homogeneous suspension of the CNTs [16]. The DEP assembly was then performed as follows: a droplet of the CNT suspension was added on top of the array, and a sinusoidal AC signal with an amplitude of 4 $V_{pk\text{-}pk}$ and a frequency of 600 kHz was applied to the electrodes through two pads on the CMOS chip, (Figure 12 (c)) to generate a positive DEP force on the CNTs. The assembly process was carried out during one hour. After DEP assembly, the chip was rinsed with de-ionized water to wash out the remaining suspension and gently dried with nitrogen. An illustration of a CNT bridging the electrode pair is shown in Figure 12 (d), the multiplexer, (MUX) has been configured to connect the corresponding electrode pairs to bias buffers and readout channels. Micrographs of the chip and a close-up of CNTs aligned between the pair of Pt electrodes are shown in Figure 13.

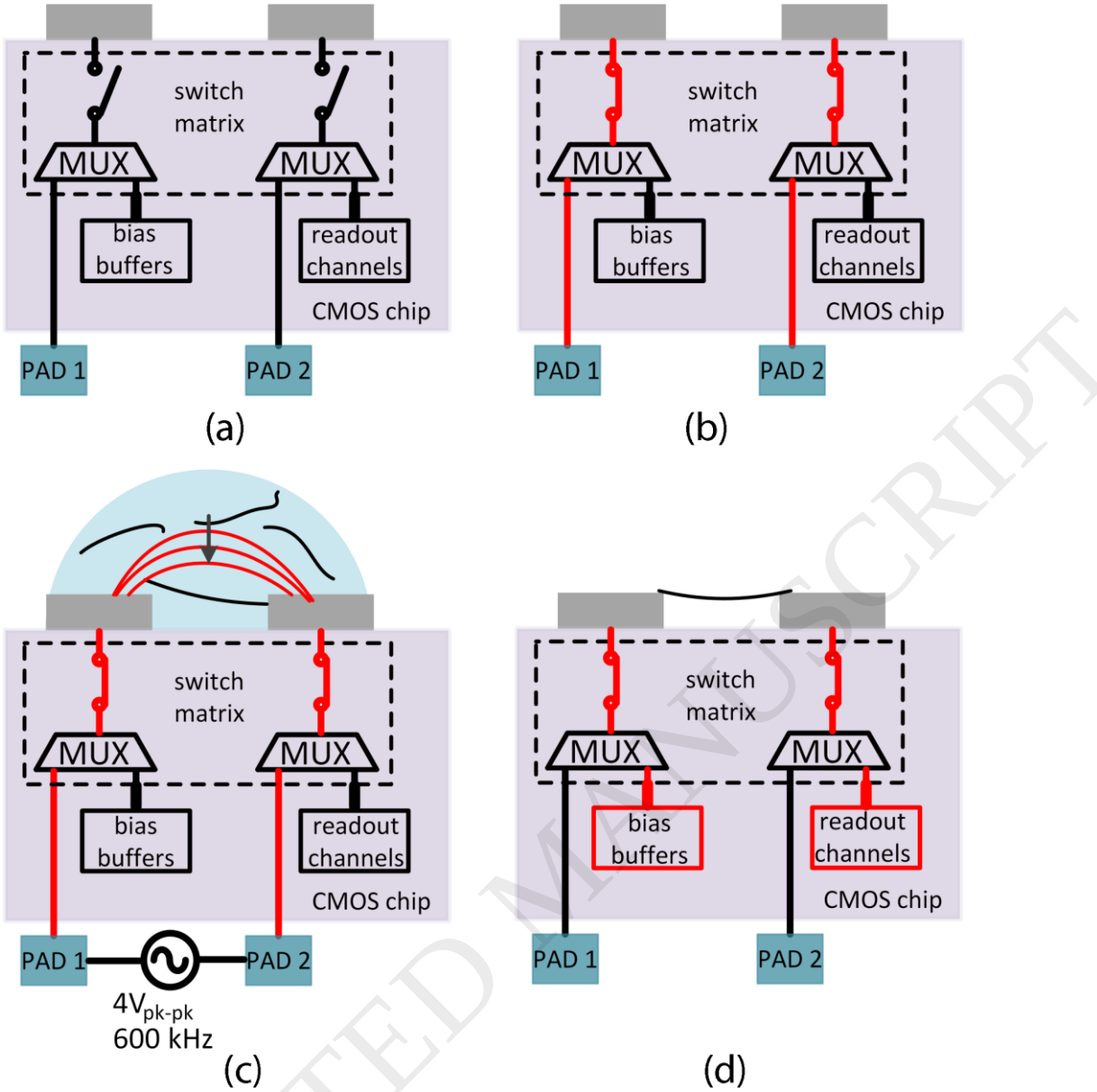

Figure 12: (a) Initial state of an electrode pair with the switch matrix underneath; (b) Configured electrode pair, wired out to two pads of the CMOS chip; (c) DEP assembly process; an AC signal is supplied by an external functional generator; (d) Electrode pair with the assembled CNT sensor; the electrodes are connected to the bias buffers and readout channels.

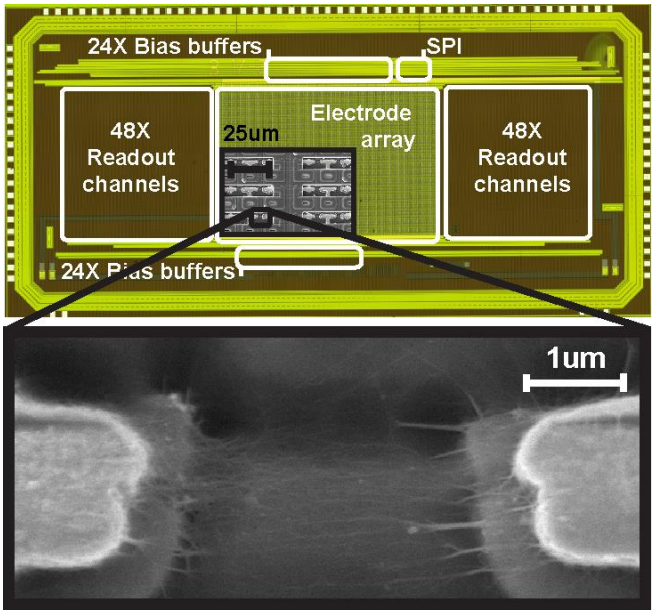

Figure 13: Chip micrograph and SEM pictures showing the array and a set of two Pt electrodes with integrated CNTs. The die size is 6.4x3.0 mm².

The possibility of performing the CNT integration via the switch matrix opens a path for realizing sensor array platforms with graded sensor sensitivity or with multiple CNT functionalization [23]. Furthermore, the CNT integration can be done after the bonding and packaging of the CMOS die and thus prevent the occurrence of damages during integration on bare silicon devices.

The integrated CNTs were then electronically characterized to determine the overall yield. On one representative chip, CNT-bridged electrode pairs were determined by electrical continuity tests performed in dry air with a 100 mV source drain potential applied across the devices. Electrode pairs were scanned with a range of gain/bandwidth settings, which ensured that devices of all conductance levels were discovered. In Figure 14 (a) the physical mapping of the devices across the whole array is shown. Due to imperfection of the packaging process, the boundary regions of the array (top and lower half left and right) were covered with some epoxy so that they were not available to the assembly process. Figure 14 (b) presents the histogram of the resistance values of the CNT devices, bridging electrode pairs, over the whole array. A dispersion of two orders of magnitudes (100 kΩ to 10 MΩ) has been observed. The epoxy-covered regions were excluded from calculation of the total assembly yield.

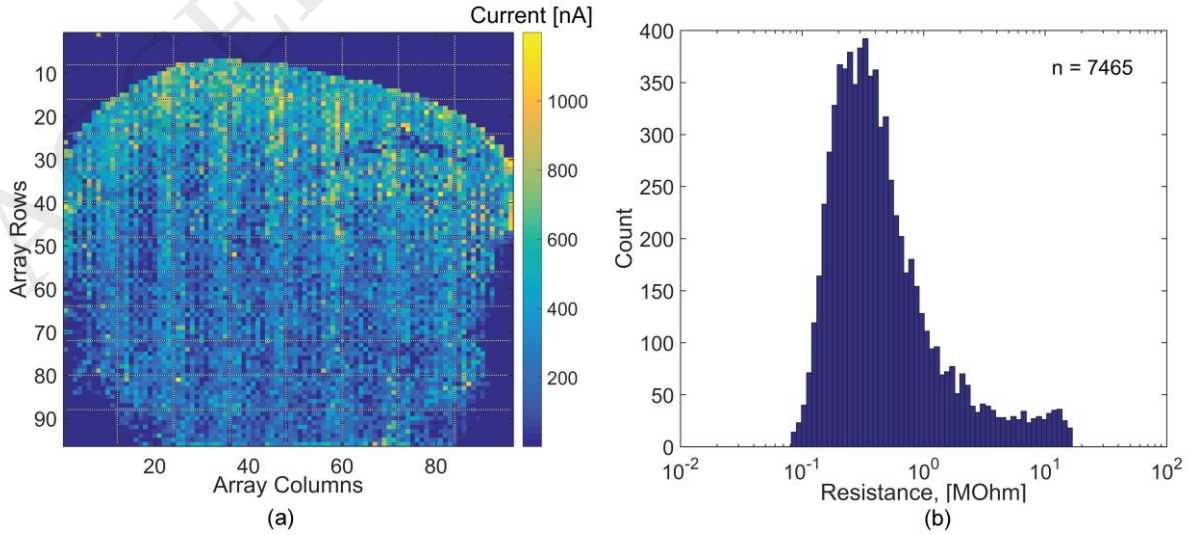

Figure 14: (a). Physical map of 7465 CNT-bridged electrode pairs detected through electrical continuity tests, (b) Histogram of resistance values over the whole array.

Sensor measurement results

To determine the variability in the electrical characteristics of the CNTFET devices connecting electrode pairs, current−voltage (IV) scans were performed in phosphate-buffered saline (PBS). The source-drain voltage was set to 100 mV, while the electrolytic gate potential was swept from −400 mV to 300 mV with respect to the source potential. The value of drain current at the gate potential of –400 mV and 300 mV was defined as I_{ON} and I_{OFF} respectively for the characterization of CNTFET devices. The ratio of I_{ON}/I_{OFF} values of each CNTFET device over the full array has been plotted on Figure 15 (a). These values can be used to deduce the nature of the devices (semiconducting or metallic). Devices with a large ratio of I_{ON}/I_{OFF} are considered to be semiconducting devices, whereas those with low ratio are metallic. As the DEP assembly has been carried out from the prepared suspension of the purchased CNT devices without any prior sorting of the CNTs, a relatively large spread of CNT characteristics has been observed. The dependence of the drain current, I, versus the potential applied through the liquid, V_{LG}, is plotted in Figure 15 (b) for the device with the highest I_{ON}/I_{OFF} ratio. The source-drain voltage was set to 100 mV.

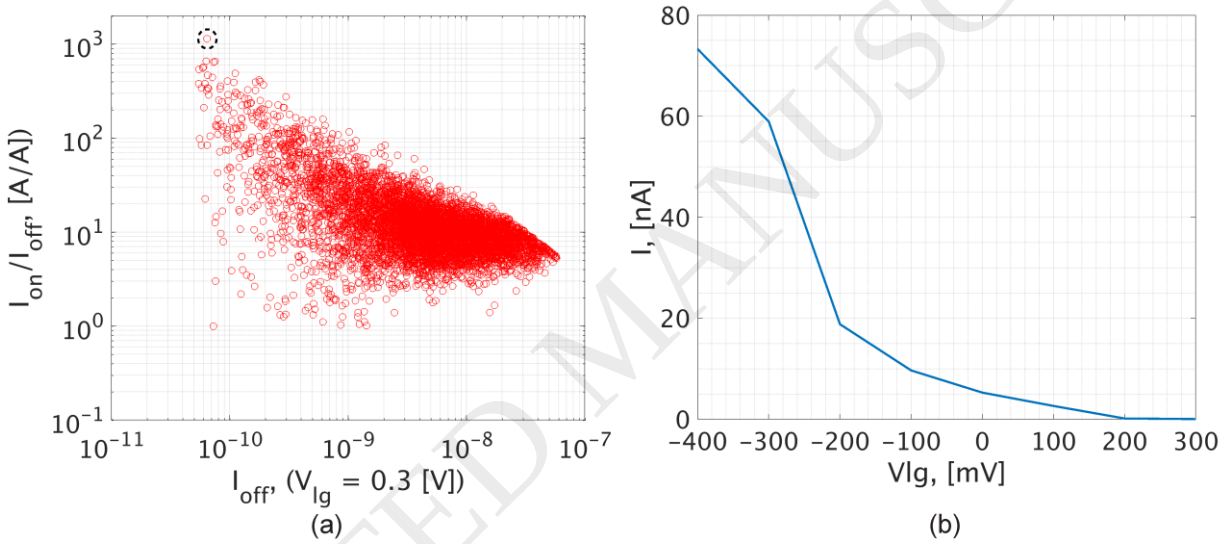

Figure 15: (a) Scatter plot of the I_{ON}/I_{OFF} ratio of all CNTFET devices of an array; (b) current−voltage characterization (I-V curve) of a semiconducting device, marked with the dashed circle on (a);

Furthermore, the CNTFETs were also characterized in terms of noise. The measurements were performed in phosphate-buffered saline (PBS) at 100 mV source-drain bias voltage and at 0 V reference voltage, provided by a low-noise Yokogawa voltage source and applied through the liquid (V_{LG}). The electrode pairs with CNTFETs have been connected to the corresponding readout amplifiers, the settings of which included a feedback gain of 106 dBOhm and a bandwidth of 1 MHz. The device current was monitored at 2 MHz sampling rate, and the noise values were calculated from 1 Hz up to 1 MHz. The results of the noise measurements of 50 devices are shown in Figure 16, together with the noise characteristics of the 10 readout amplifiers. The noise from amplifiers starts to dominate the noise of the CNTs at the frequencies greater than 100 KHz, which causes instrumentation-based degradation of the signal-to-noise ratio. As has been reported before, CNTs exhibit an 1/f noise spectrum across the entire measurement bandwidth [24]. The large spread in the CNTFET noise can be explained by a large spread in the initial CNT resistances or conductances. According to Collins et al, [24], the amplitude of the 1/f noise is inversely proportional to the number of charge carriers, N_C, in the nanotube and, consequently, inversely proportional to the conductance, G, of the CNT. N_C and G depends on the number of parallel CNTs that form connections between a given electrode pair. Due to the statistical nature of the dielectrophoresis assembly process, the number of parallel CNTs between

electrodes can vary from a few to a whole bundle of CNTs. Therefore, a conductance dispersion over a few orders of magnitudes is expected and observed, which entails a large spread in the noise characteristics. The average value of measured I_{rms} from a 50 CNTFETs at the bandwidth of 1 MHz was equal to 4.9 nA_{rms}. The average noise of the amplifier, connected to an electrode and integrated from 1 Hz up to 1 MHz bandwidth, was 0.84 nA_{rms}, which means that the CMOS circuitry is not limiting the performance of the CNTFETs.

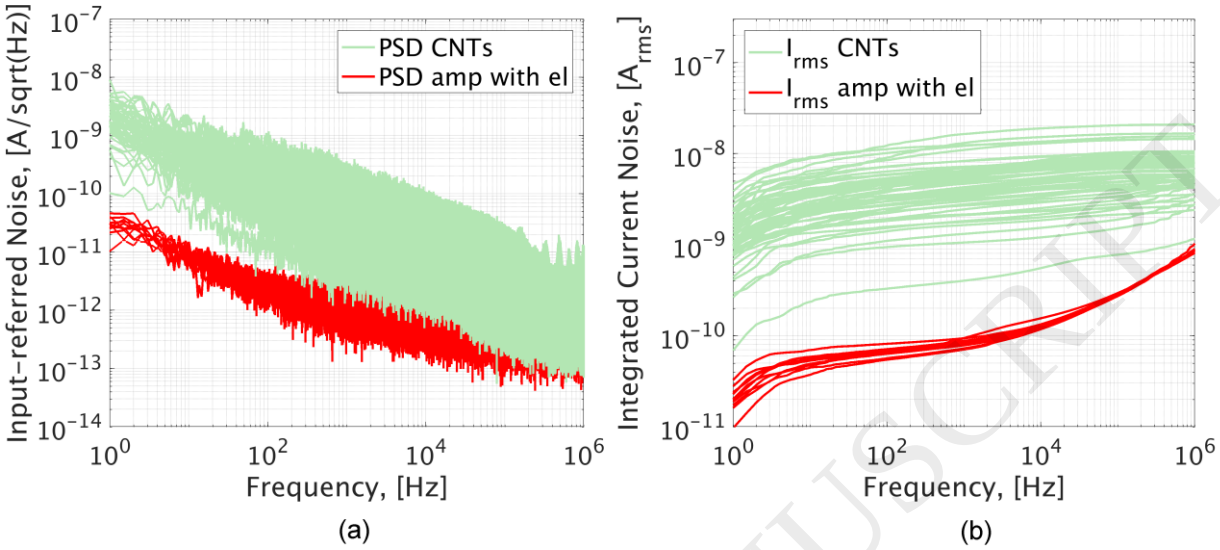

Figure 16: (a) Input-referred power spectral density (PSD) of 50 CNT devices (green) and an amplifier (red), connected to an electrode in phosphate-buffered saline (PBS); (b) Integrated current noise of the corresponding PSD curves.

The validation of the sensing capabilities of the CNT devices in liquid phase has been done by carrying out measurements of different pH values. Sodium-citrate and sodium-phosphate buffers with pH values from 3 to 8 were prepared. During the measurements the source-drain voltage of CNTFETs was set to 100 mV, whereas the electrolytic gate potential was set to -300 mV.

The CNTs used in this paper were single-walled CNTs with carboxylic-acid functionalization. The carboxyl functional groups, (-COOH), located at the surface of CNTFET devices modulate their conductance upon exposure to different pH values due to protonation or deprotonation of the functional carboxyl groups.

First, we studied the behavior of the CNTFET sensors over the full array. We measured the CNTFET resistance upon exposure to solutions between pH=3 and pH=8. The resistance generally decreased with increasing pH-value. We then used the resistance value at pH=3 as a reference value. The resistance ratio, R_{pH3}/R_{pH8}, was then plotted versus the respective reference resistance values, R_{pH3}, in Figure (a). It has been observed that the resistance changes of the CNTFET devices upon an increase of the pH value depended on the initial or reference resistance of the CNTFET devices, and that R_{pH3}/R_{pH8}-ratio values ranged between one and approximately 2.5. The CNTFET devices with higher initial resistivity also exhibited higher resistance changes upon increasing the pH-value. The distribution of the CNTFET R_{pH3}/R_{pH8}-ratio values is shown in Figure (b). The average value amounted to 1.35.

The scaling of the minimal resolvable pH-value increment with the number of used CNTFET sensors has been plotted in Figure (c). The measured data were recorded at 4 kHz sampling rate from one randomly selected 12x8 block out of whole CNTFETs array (96 CNTFETs in total) over entire pH range. CNTFETs response to every pH value have been recorded for approximately 15 seconds. Following this step, data were low-pass filtered up to the bandwidth of 100 Hz. The Fisher information for every pH value has been estimated, including the calculation of the covariance matrix for all 96 CNTFETs. Fisher information describes the variance of the mean value of the measured experimental dataset. Finally, the resolution was defined, based on Cramer Rao bound, as the inverse of the square root of Fisher information. The minimal resolvable pH-change value for using a single CNTFET device was estimated and measured to be 0.2 pH-units (Figure 17 (e) and 17(f)) in the

middle of pH range, while, upon using an average value from up to 96 CNTFETs, the noise in the signals drastically decreased due to their uncorrelated nature, and the minimal resolvable value amounted to 0.025 pH-units. This is a good resolution and approximately one half of the detection limit that has been reported in [25]. The averaged normalized current response (normalization: the initial current at pH 3 was set to one) of 96 CNTFET devices over a range of pH values is shown in Figure (d). The solutions with different pH-values were applied sequentially to the microfluidic chamber, starting from 3 up to 8 and back to 3 to show the signal reversibility and sensor performance. The temporal characteristics reflect that of the measurement chamber and not of the devices. The response time of individual sensors to a pH change is on the order of ~1 second.

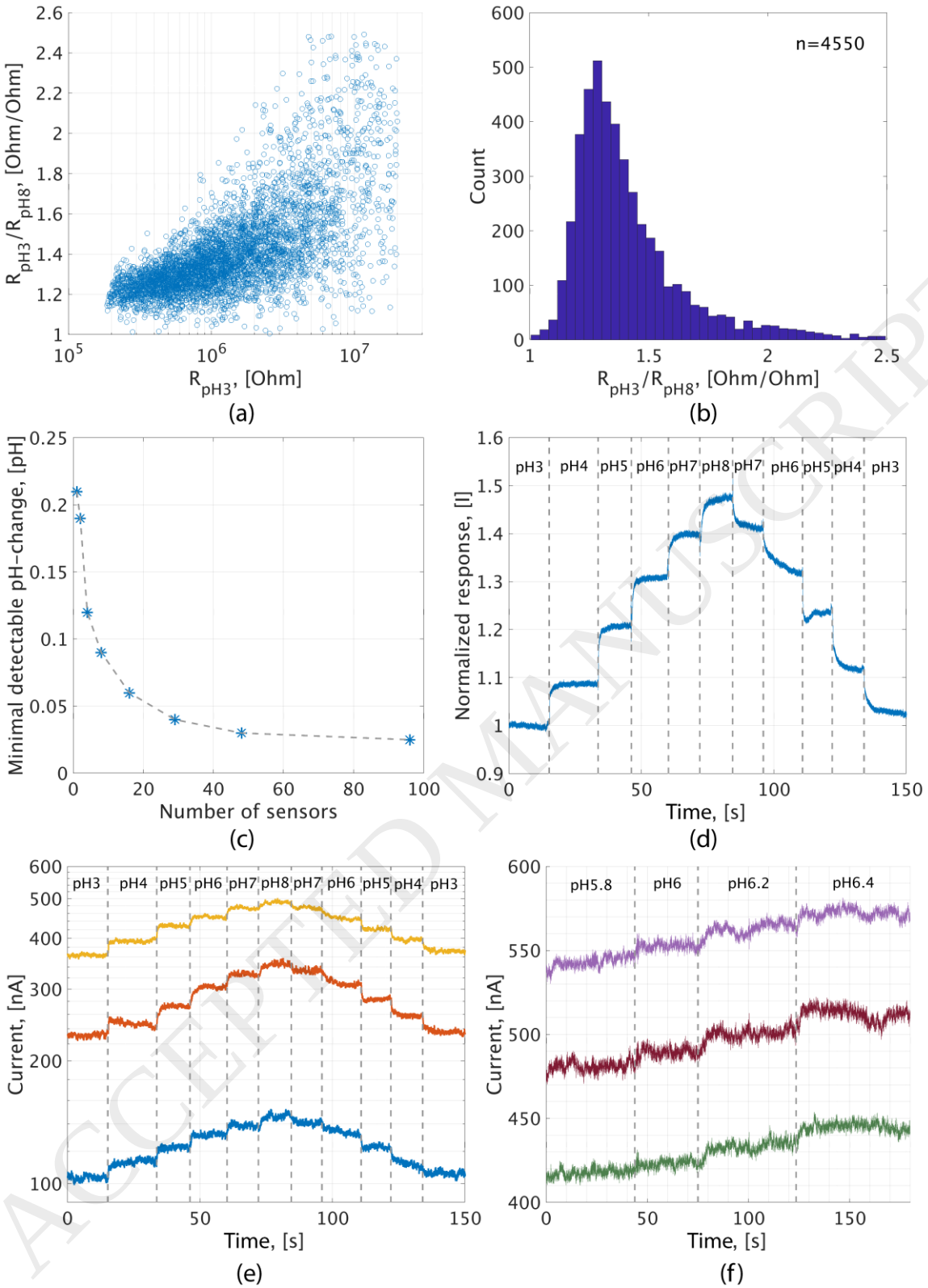

Figure 17: (a) Scatter plot of the relative change of the CNT resistance ratio R_{pH3}/R_{pH8} versus the respective initial resistance values, R_{pH3} ; (b) Histogram of the R_{pH3}/R_{pH8} resistance ratio of all CNTs of the array; (c) Scaling of the minimal resolvable pH-change with the number of used CNTFET devices; the respective sensor signals were averaged; (d) Normalized, averaged current response, [I], of 96 CNTFET devices upon sweeping the pH values from 3 to 8 and back to 3. (e) Current changes versus time of 3 different CNTFET devices upon sweeping the pH values from 3 to 8 and back to 3; (f) Current changes of another 3 individual CNTFET sensors upon small pH variations in 4 steps from 5.8 to 6.4.

In Figure 18 (a) the calibration curve of the averaged normalized current response of 96 CNTFETs over a pH range from 3 to 8 is shown. The average non-linearity over the 96 CNTFETs amounted to approximately 2%. The drift of one randomly selected CNTFET (top trace displayed in orange color in Figure 17 (e)) during 10 seconds is shown in Figure 18 (b) for the different applied pH values. The current was normalized (normalization: the initial current at pH 3 was set to one). The different traces show the drift characteristics at pH values from 3 (dark blue) at the bottom to 8 (light blue) at the top. A linear fitting for each trace has been performed, and the corresponding drift for each pH value has been estimated as relative pH change per second. The average drift over the whole pH range of 3 - 8 was approximately 0.01pH/s. For longterm pH monitoring, a re-calibration of the CNTFET sensors may be required.

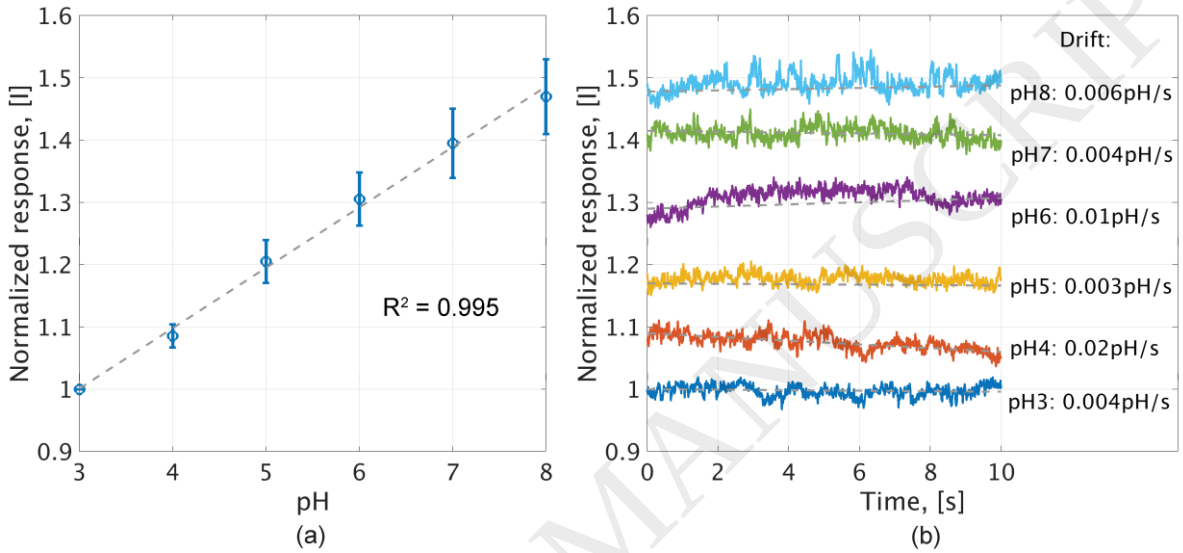

Figure 18 (a) Calibration curve of 96 CNTFETs in a pH range between 3 and 8. Nonlinearity was approximately 2%; (b) Drift characteristics (relative drift) of an individual CNTFETs during 10 seconds. The different traces show the characteristics at different pH values from 3 (dark blue) at the bottom to 8 (light blue) at the top.

One potential application of the designed sensor system is the measurement of ion concentration gradients. Ions play a crucial physiological role in a large number of cellular processes. The mis-regulation of local ion concentrations is suspected to be an indication or cause of various diseases including, e.g., epilepsy or Alzheimer's disease [26,27]. Monitoring of local ion gradients in system such as dissociated brain culture cells could, therefore, principally improve detection or diagnosis of such diseases. Normally, the Na+ concentration is 140 mM outside of the cell and 10 mM inside. The K+ concentration is 140 mM inside and around 20 mM outside the cell [26]. Since the ionic regulation takes place at cellular level, the sensing unit is required to have a length scale comparable to that of the cells, i.e., µm-scale or smaller. Furthermore, as physiological processes typically involve different ionic species, it would be beneficial that the sensing device would be capable of specifically detecting certain ions or even multiple ions in parallel.

Here, we have performed proof-of-concept measurements of the response of CNTFET sensors to different concentrations of NaCl. The same microfluidic setup as for the measurement of different pH response has been used.

The results obtained from 96 CNTFETs have been plotted in Figure 19. The presence of Na^+ ions in the solution has a similar effect on the CNTFETs as applying a positive gate voltage, so that the CNTFET resistance increases with increasing concentration of NaCl. The normalized current changes as a function of a $1/\log_2$ of a target NaCl concentration, Figure 19 (a). The measurements were performed in a sequence, starting with a concentration of 1 mM, then applying 10 mM, back to 1 mM, then increasing the concentration to 40 mM and so on, see Figure 19 (c). Again, the referencing to the initial current values was necessary,

as the zero-exposure resistance values of the individual sensors varied over a large range (single CNTs, multiple CNTs, and different characteristics). The distribution of the ratio of the CNTFET resistance values, $R_{160mM\ NaCl}/R_{10mM\ NaCl}$, is shown in Figure 19 (b). The average ratio value amounted to 1.16. The normalized, averaged CNTFET resistance changes upon applying different NaCl concentration is shown in Figure 19 (c). The averaging has been performed over 96 CNT sensors. The minimal resolvable NaCl - concentration change for one CNTFET device was estimated to be 40 mM of NaCl in the range of concentrations between 80 mM and 320 mM, while, upon using an average value from up to 96 CNTFETs, this minimal resolvable value decreased to 4 mM of NaCl.

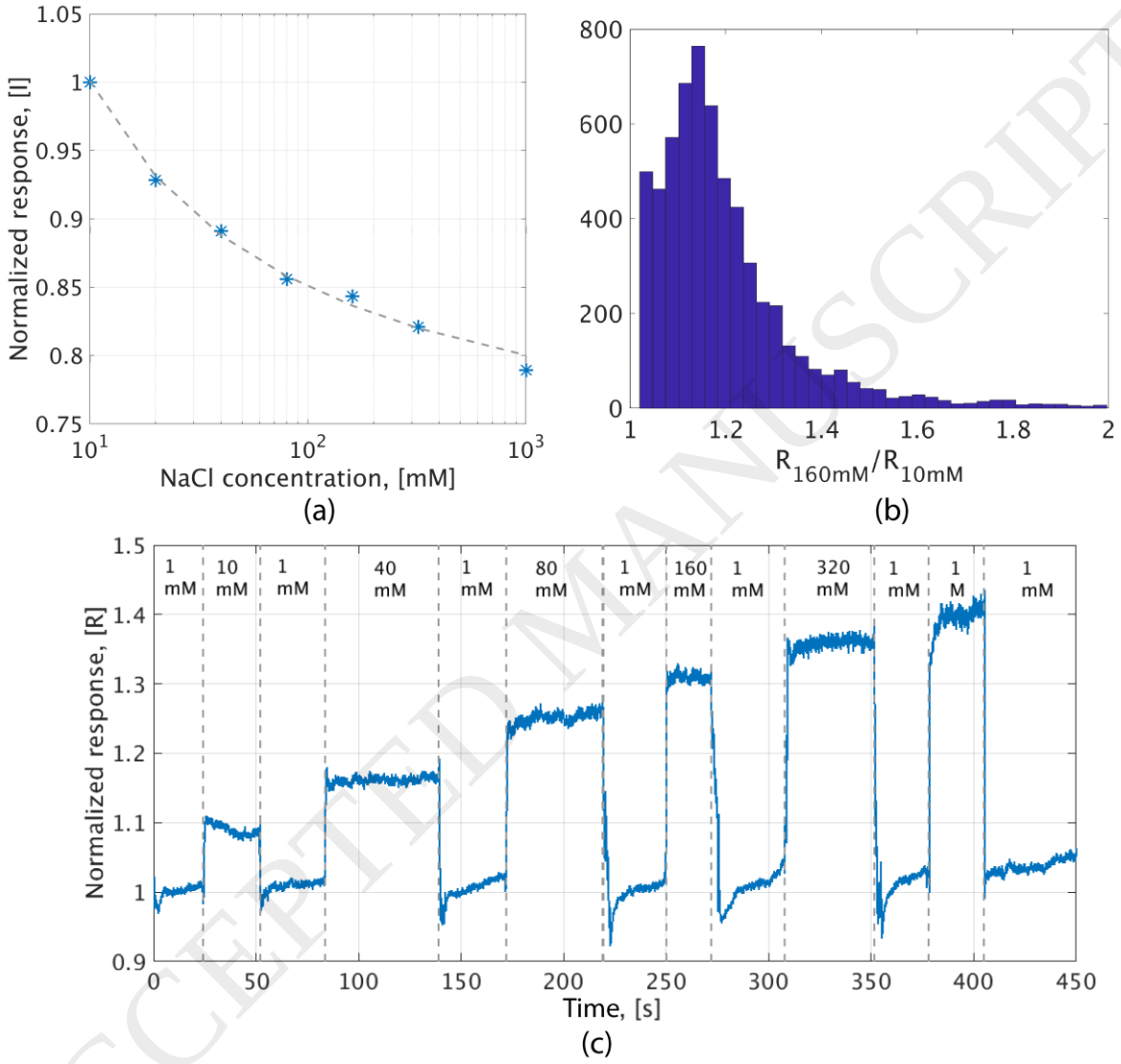

Figure 19: (a) Normalized device current calibration curve, [I], for different concentrations of NaCl; the graph shows the average of 96 CNT devices, the normalization was done with respect to the starting value for 10mM of NaCl. (b) Histogram of the ratio of the resistance values R_{160mM} and R_{10mM} of all CNTs of the array; (c) Normalized resistance changes, [R], versus time upon sweeping the NaCl concentration from 1 mM to 1 M; the displayed values represent the average over 96 sensors; normalization was done with respect to the initial resistance values upon exposure to 1 mM NaCl.

Conclusion

We have presented a monolithic sensor system featuring an array of 9,216 CNTFETs along with 96 integrated readout and amplification channels. The array was designed using a switch-matrix approach, where certain number of sensors could be selected from the array and wired out to the readout channels. Readout channels were realized with low-noise and

wide-bandwidth trans-impedance amplifiers, which enabled measurements in a bandwidth between 1 Hz and 1 MHz and to determine current values in the pA to µA range. The achieved noise value over a bandwidth of 1 KHz was 2.14 pArms, which is comparable to other state of-the-art systems. The noise value over a bandwidth of 1 MHz was measured to be 0.84 nA. An effective CNT integration into large-scale and high-density arrays has been achieved by applying dielectrophoresis-based methods and utilizing the capabilities of the switch-matrix on the CMOS chip. The functionality of the circuits and system has been verified through measurements of CNTFET responses to solutions of different pH values. The smallest resolvable pH-change value has been estimated to 0.025 pH-units, which is the smallest value reported so far. Moreover, CNTFET responses to sodium chloride (NaCl) concentration changes have been shown. The designed system is able to detect changes in NaCl concentration within the physiological range of living cells. The smallest detectable value for NaCl concentration changes has been estimated to be equal to 4 mM NaCl. We believe that such highly integrated sensor systems may prove to be useful for the detection of different analytes at high spatial and temporal resolution and sufficient sensitivity.

Acknowledgements

The authors would like to acknowledge the ZMB (Zentrum für Mikroskopie) of the University of Basel, Switzerland, for taking the SEM pictures and Dr. Felix Franke, BEL, ETH Zürich, for help with data analysis. Financial support through the Riken program for Junior Scientists, Japan Society for Promotion of Science (JSPS) under Grants–in-Aid for Young Scientists or KAKENHI (B) (No. 26790035) and the European Union ERC Advanced Grants “neuroXscales”, contract number AdG 694829 (H2020), and "NeuroCMOS", contract number AdG 267351 (FP7) is acknowledged.

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