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High-Temperature Annealed Flexible Carbon Nanotube Network Transistors for High-Frequency Wearable Wireless Electronics

Yu Lan, [†, §, #] Yang Yang, [‡, #] Yan Wang, [†] Yun Wu, [‡] Zhengyi Cao, [‡] Shuai Huo, [‡] Lihong Jiang, [‡] Yunchuan Guo,[†] Yunqiu Wu, [†] Bo Yan, [†] Ruimin Xu, [†] Yuanfu Chen, [†, ¶] Yanrong Li, [†] Shalini Lal, [§] Zhenqiang Ma, [§,*] & Yuehang Xu[†,*]

[†]School of Electrical Science and Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan, 611731, PR China

[‡]Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing Electronic Device Institute, Nanjing, Jiangsu, 210016, PR China

[¶]Department of Physics, School of Science, Tibet University, Lhasa 850000, PR China

[§]Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, WI, 53705, USA

[#] Y. Lan and Y. Yang, contributed equally.

[*]Authors to whom correspondence be addressed to Z. Ma (email: mazq@engr.wisc.edu) and Y. Xu (email: yuehangxu@uestc.edu.cn)

ABSTRACT

Semiconducting single-walled carbon nanotubes (SWNTs) are potential active material for fast-growing flexible/wearable applications with low power dissipation, especially suitable for increasingly important radio-frequency (RF) wireless biosensor systems. However, the operation frequency of the existing flexible carbon nanotube field effect transistors (CNT-FETs) are far below the current state-of-the-art GSM spectrum frequency band (typical 850 MHz) for near-field wireless communication applications. In this paper, we successfully conduct a 900 ℃ annealing process for the flexible CNT-FETs and hence significantly improves their operation frequency up to 2.1 gigahertz (GHz), making it possible to cover the current GSM spectrums for integrated wireless sensor systems. The high-temperature annealing process significantly improves the electrical characteristic of the flexible CNT-FETs by removing the surfactant impurities of the SWNTs materials. The obtained flexible CNT-FETs exhibit record transconductance (g_m) as high as 48 μS/μm. Despite an applied strain level of 2%, a characteristic frequency of over 1 GHz is observed. Further demonstration of GHz performance is also exhibited for flexible RF integrated circuits (ICs) such as frequency multipliers and mixers, which are the fundamental components for wireless applications. This work offers a new pathway for realizing SWNTs-based wearable wireless GHz sensor systems with power-efficiency.

KEYWORDS

Flexible wearable electronics, High-temperature anneal, Nano-membrance transfer technique, Wireless applications, Radio-frequency integrated circuits, Carbon nanotube transistors.

INTRODUCTION

Because of high mobility, near-ballistic transport and low-intrinsic capacitance, single-walled carbon nanotubes (SWNTs) have been presented as promising semiconducting materials to achieve high-performance transistors with low power dissipation. [1-9] In recent report, CNT-FETs with a 5 nm gate length (L_g) have been shown, which indicates that the energy dissipation even reaches the quantum limit of a binary switch.[10] Very recently, CNT-based Si complementary metal-oxide-semiconductor (CMOS) chips are used for GHz wireless sensor systems, showing energy efficiency and high sensitivity. [11] Much lower power dissipation makes the CNT-based ICs attractive for biosensors, microprocessor and Internet-of-Thing (IoT) devices and systems.

Furthermore, the SWNTs are also suitable for flexible/wearable devices due to the low power dissipation and excellent mechanical (fracture strain up to 30 %) properties. The heat dissipation issue is always a big challenge for flexible electronics. In the last decade, flexible CNT electronics have achieved great progress, [12-20] but still face challenges to get operation frequency over GHz on bendable substrates, which limits their applications in near far-filed wireless communications such as the GSM applications. Although great progress has been achieved for high-speed flexible CNT-FETs,[21,22] the highest maximum oscillation frequency (f_{max}) is 140 MHz, which is still not high enough for the GSM spectrum. The f_{max} represents the maximum work frequency that can get power amplification. Thus, the primary task is to increase the frequency of flexible CNT-FETs up to GHz range and realize GHz ICs.

Current state-of-the-art flexible SWNTs electronics are mainly fabricated by directly depositing the SWNTs networks onto plastic substrates through dielectrophoresis (DEP)[21] and/or drop spinning methods.[12-20, 22] These deposition methods can't remove surfactant impurities in SWNTs,

which primarily affects their electrical properties. Then, it is imperative that a fabrication method should be developed to mitigate such contaminants on flexible substrates. It is well-known that high-temperature annealing process is a simple and efficient way to eliminate the residual surfactant.[11,23-25] However, the high-temperature annealing process is not compatible with flexible electronics, because the plastic substrates can't withstand high temperature.

In this paper, we successful develop a thermal annealing process at 900℃ to remove the residual surfactants in SWNTs networks on plastic substrates. Finally, we present the GHz flexible CNT-FETs with a record f_{max} of 2.1 GHz, which fully cover the GSM spectrums. Such high-performing flexible CNT-FETs are used to design integrated circuits applications that comprise of GHz frequency multipliers and mixers, which are the fundamental components in future flexible/wearable wireless communication systems such as RFID and wireless GHz sensor array.

EXPERIMENTS and FABRICATION

Development of a thermal anneal and Au nano-membrance transfer method

The main impurities in our IsoNanotubes-S SWNTs samples include metal catalyst (1% by mass), surfactants (iodine 5% by mass) and carbonaceous, which cannot be removed by surfactant removal procedures.[26] In other cases, the metal catalysts, carbonaceous materials and surfactants impurities dispersed in nanotube solution could also be deposited on the target substrates with useful semiconductor SWNTs. High-temperature anneal is normally used for SWNTs film surface treatment in order to improve their RF performance on rigid applications. But the challenge arises in that flexible electronic devices generally have a low thermal budget in fabrication processes.

Herein we develop a novel annealing and transfer strategy to make the high-temperature process compatible with the low-temperature fabrication requirement of flexible CNT-FETs. The SWNTs films are firstly deposited onto a rigid silicon (Si) wafer for the high-temperature processes. To avoid the useful semiconductor SWNTs decomposition in ambient air at high temperature, we employ a mixture of 5% hydrogen (H_2) and 95% argon (Ar) as protective gases for the annealing process at 900℃ in a sealed chamber. This thermal anneal significantly purges the surfactant (5% iodine by mass) and carbonaceous impurities from semiconductor SWNTs (shown in Supporting Information Figure S2). After the annealing process, the SWNTs films are delaminated from the Si wafer and then transferred onto flexible polyethylene terephthalate (PET) substrates at room temperature (shown in Figure 1).

The Au nano-membrance transfer method is another key development step towards fabricating the flexible GHz CNT-FETs. It serves three purposes, firstly, it acts as a transfer-supporting layer and, secondly, it forms the self-aligned ohmic contact electrodes and lastly, it protects the SWNTs films from photoresist and other organic contamination during the upcoming fabrication processes.

Preparation and transfer the SWNTs onto flexible substrates

Figure 1 shows how the SWNTs are prepared and transferred onto a flexible PET substrate. A 500 nm amorphous silicon dioxide (SiO_2) is firstly deposited on a 500 μm silicon wafer through plasma-enhanced chemical vapor deposition (PECVD) method. The SiO_2 layer acts as a sacrificial layer to enable SWNTs transfer in a latter step. The SWNTs are then deposited onto the SiO_2 surface (via drop cast and spin coating, as shown in Figure 1.a). The nanotube suspension solution is a commercially available dispersed solution with 0.01 mg/mL high-purity semiconducting nanotubes (99%), which comes from NanoIntegris, Inc.[26] After the spin-coating process, the

SWNTs are annealed at 900℃ in an Ar and H_2 ambience for 6 hours (Figure 1b). A Raman spectrum with a narrow G-peak (inset of Figure 1a) implies that the annealed SWNTs are still semiconducting after annealing at 900 ℃ for 6 hours. The nanotube is about 1~2 μm in length and the nanotube density is about 16 tubes/μm (shown in Supporting Information Figure S4). A 50-nm Au nano-membrance is deposited on the surface of the SWNTs (Figure 1c). At the end of this step, the layer structure comprises of Au/SWNTs/SiO_2/Si from top to bottom.

To delaminate the SWNTs films from the rigid Si wafer, we use 10% hydrofluoric acid (HF) solution to undercut the sacrificial SiO_2 layer. This is achieved by placing the sandwich structure (Au/SWNTs/SiO_2/Si) on the surface of the HF solution (Figure 1c, left), which etches the SiO_2 layer from the edge of the floating structure. The water surface tension aids in separating the Au/SWNT films and Si wafer, with the result that the Au/SWNT films float on the surface while sinking the Si wafer in the HF solution. Finally, the Au/SWNT films are transferred onto PET substrates (Figure 1d). Bonding between the SWNTs film and PET substrate is obtained by baking at 100℃ for 12 h.

Fabrication of flexible nanotube FETs

Figure 2 illustrates the process flow for fabricating the flexible CNT-FETs on PET substrates with a thickness of 150 μm. The SWNTs thin films, which are covered with a 50-nm-thick Au film, are first transferred onto a PET substrate (Figure 2a). Thereafter, standard lithographical method is employed to isolate the channel regions of the CNT-FETs. The Au nano-membrane outside the channel areas are etched away using aqueous KI: I_2 solution, followed by photo-lithography and Au wet etching solution to define the gate channel length (1.5 μm) (Figure 2b). The ungated gold films outside the gates areas also act as the self-aligned source/drain ohmic

contacts. An 8-nm-thick Al_2O_3 is deposited by atomic layer deposition (ALD) as gate dielectric, and Ti/Au (30 nm/550 nm) metal film is deposited through e-beam evaporation as top-gated electrodes (Figure 2c). This self-aligned process forms the well-aligned Al_2O_3/gate metal structure, which effectively insulates gate electrodes from drain and source electrodes.[27] The fabrication flow is completed by an additional metal evaporation of Ti/Au (30 nm/200 nm) layer to thicken the drain and source electrodes pads, which are designed using a 150 μm ground-signal-ground (GSG) coplanar waveguide (RF test pads of the flexible RF transistors) for RF probe tests. Thick gate metal electrodes decrease the gate resistance and further improves its RF performance, mainly the maximum available power gain. The G-S-G coplanar waveguide design not only extends the source/drain contact area but also optimizes the heat dissipation capacity of the flexible CNT-FETs. More details about the fabrication processes are shown in Supporting Information Figure S5.

Figure 3 shows an optical micrograph, SEM and the cross section focused ion beam (FIB) images of the designed flexible CNT-FETs. Figure 3a demonstrates a camera image of CNT-FETs arrays on a bendable PET substrate with 20 cm × 20 cm dimensional size. Figure 3b shows a 4 × 6 array for the flexible CNT-FETs. The CNT-FETs consist of two-finger top-gated active channels (Figure 3c). Figure 3c shows the gate architecture of the device with a gate length of 1 μm, while Figure 3d shows that the length of the access region (or the ungated area) is approximately 500 nm. The contribution of access region length as well as the gate-length equals a total channel length of 1.5 μm for a CNT-FET.

The 500 nm wide access region is a result of an unintentional lateral etching during the wet etch process. There is a trade-off between the thickness of the source/drain ohmic contacts (thickness of the Au nano-membrance used for transfer) and the ungated access length; a thicker source/drain

contact yields lower parasitic resistance. However, thicker gold nano-membrances increase the wet etch time, thereby widening the lateral undercut and the ungated channel length. In addition, the Au nano-membrances that are too thin (typically below 30 nm) have low survival rate during the wet transfer process, as shown in Figure 1c. A thickness of 50 nm has been found to limit the lateral undercut and its access region resistance while achieving a good transfer survival rate.

RESULTS and DISCUSSION

DC and RF Performance of the Flexible CNT-FETs

Figure 4 shows the measured direct current (DC) characteristics of the flexible CNT-FETs under different bending conditions (flat, ε=1.5 % and ε=2 %). The tensile strain level is calculated from the curvature radius, which is given by $\varepsilon = t/(t + 2r)$, where r (r=5 mm for 1.5% and r=3.75 mm for 2%) represents bending radius of the measuring vehicle and t represents the thickness of the flexible PET substrates. The insets in Figure 4a-c represents the drain-source resistance characteristics (R_{ds}) of the CNT-FETs at a drain voltage of −3 V, with V_g of −1 V to 1 V for each three different bending conditions of 0%, 1.5% and 2%, respectively. The rise in strain causes an increase in R_{ds}. This is mainly due to a rise in the ohmic contact resistance and access resistance with the increasing stress applied to flexible substrates (as shown in Figure 4d).

Figure 5 shows the RF characteristics of our flexible CNT-FETs. A g_m of 48 μS/μm is measured. To the best of our knowledge, this g_m is 40 times higher than the previous highest reported value g_m=1.2 μS/μm for flexible CNT-FETs. The f_T and f_{max} are extracted from the S-parameters and serve as main performance indices for high-frequency transistors. We measured the S-parameters

from 0.1 GHz to 5 GHz at 50 MHz steps using G-S-G RF probes station and a vector network analyzer. To evaluate the practical transistor characteristics in real microwave circuits, de-embedding is achieved by using customized pad de-embedding open-short dummy structures (Supporting Information S6). This involves removing the bonding test pad effects to reveal the real transistor's RF performance without test pads. After the pad de-embedding, the f_T and f_{max} increases by about 20 % (Figure 5c, d). It is noted that the contributions from gate fringe capacitances between the gates and source/drain electrodes are unaffected by pad de-embedding.

A record extrinsic f_T and f_{max} of 1.9 GHz and 2.1 GHz, respectively, are achieved for the flexible CNT-FETs with a 1.5 μm channel length (Figure 5c, d). The f_{max} of 2.1 GHz reported here is an order of magnitude faster than existing flexible CNT-FETs[21,22] and other organic solution-processed transistors.[28-37] For RF circuits, the power gain is an important figure of merit (FOM) for real RF circuits; it defines the ability of power magnification at radio frequencies. The maximum stable gain (MSG) (marked by the pole transition point of 1.9 GHz in Figure 5c) indicates the available power gain if suitable input and output matching networks are employed for an unconditionally matched amplifier design. The MSG of the designed flexible CNT-FETs is about 6 dB at 1 GHz. This indicates that our flexible CNT-FETs could be used to design RF amplifiers in the GHz regime. This MSG level is comparable with solution-processed flexible Ⅲ-Ⅴ (InAs nanowire) thin-film transistors.[34] The f_{max} and f_T have a typical relationship of $f_{max} = f_T/\left(2\left(g_d(R_{ps}+R_{gate})+2\pi f_T C_{p,gd} R_{gate}\right)^{0.5}\right)$,[6] where the g_d is the drain conductance, R_{gate} is the gate resistance, R_{ps} is the parasitic series resistance for source, and $C_{p,gd}$ is the parasitic gate drain capacitance. In this work, the improvement in f_{max} is achieved primarily on account of the following three factors. (a) The use of commercially available ultra-high pure semiconducting nanotubes (99.9%) that enable reduction in drain conductance (g_d), (b) High temperature anneal

and Au transfer that reduces parasitic resistance (R_{ps}), and the thick gate metal reduces the gate resistance (R_{gate}). (c) Applying spin coating multiple times, specifically, three times, that increase the density of nanotubes, which increased density reduces ($C_{p,gd}$).

The effective field mobility can be deduced by the equation: $\mu_{FE} = (L_{ch}g_m)/(W_{ch}C_{ox}V_{ds})$). The g_m represents the measured transconductance (g_m = 48 μS/μm) at a bias voltage, V_{ds} of −3V, W_{ch} represents the effective channel width (2 × 60 μm)， C_{ox} represents the actual gate capacitance (about 4.8×10^{-13} F), and L_{ch} represents the channel length (1.5 μm). The actual C_{ox} is calculated using the tested $f_{T,intrinsic}$ and g_m ($f_{T,intrinsic}=g_m/(2\pi C_{ox})$),[4] more details are shown in supporting information Section S9. The actual μ_{FE} is deduced to be approximate 60 cm^2/ (V. s), which is the highest mobility for flexible RF CNT-FETs. The record high RF characteristics obtained herein confirm that the experiments of high temperature annealing and Au film transfer can significantly enhance the RF performance of flexible CNT-FETs.

Table 1 summarizes the RF performance metrics of "f_T," "f_{max}" and "$f_{max} \times L_{ch}$" for different state-of-the-art flexible nanomaterial systems, such as, CNT-FETs, graphene, black phosphorus (BP), MoS_2, and Ⅲ-Ⅴ Indium arsenide (InAs) nanowires). With different L_{ch} for different devices shown in Table **1**, it is preferable to compare the FOM of "$f_{max} \times L_{ch}$" to evaluate different types of thin-film transistors. The FOM ($f_{max} \times L_{ch}$) of 3.15 GHz × μm is demonstrated for the solution-based flexible CNT-FETs shown in this work. This is not only an order of magnitude higher than the record FOM for flexible CNT-FETs (0.36 GHz × μm) but also comparable with other 2D materials (mechanically exfoliated BP: 5.15 GHz × μm; CVD MoS_2: 2.1 GHz × μm, and CVD graphene: 8.4 GHz × μm) and III-V nanowire transistors (InAs nanowire: 2.7 GHz × μm). Despite the fact that graphene and InAs III-V thin films are limited in real flexible applications due to the

lack of a bandgap and intrinsically low strain, respectively, the RF performance of graphene and InAs-based flexible transistors is also summarized in Table **1** for benchmarking state-of-the-art flexible high-frequency transistors. From this comparison, SWNTs shows significant potential as a promising material for flexible/wearable RF nano-systems and applications.

To assess the mechanical stability and reliability of our flexible CNT-FETs, we tested its RF performance under different strain levels, as presented in Figure 6. The tensile strain is applied along the channel direction by sticking the device to the surface of a semi-cylinder sample holder (see inset of Figure 6d). Panels a–c in Figure 6 show the RF characteristics of the CNT-FETs at strain levels of 1.5%, 2% and 3%, respectively. The f_T and f_{max} are extracted from the measured S-parameters at different bending conditions. Figure 6d shows stepwise variation in the f_{max} under different strain levels and after releasing the strain, which indicates that the f_{max} degrades insignificantly (<20%) as the strain is increased to 2% and on releasing this strain, the f_{max} values recover to within 80% of that without the strain. This recoverable f_{max} after bending behaviors indicates that our flexible CNT-FETs are reliable against repeatable bending conditions. However, on increasing the strain further (beyond 3%), a permanent drop of about 80% in f_{max} is observed (see Figure 6d).

Flexible nanotube Microwave-Frequency multipliers and mixer

The record-high g_m and an operating frequency range in GHz demonstrated in this work make CNT-FETs as a suitable candidate for microwave applications on flexible substrates. CNT-FETs can be used to design frequency multipliers and microwave mixers[38-40] due to the nonlinear response I-V characteristics. Such a GHz frequency multiplier is designed as shown in Figure 7a. When the input RF signal is a sinusoidal function wave with frequency w ($V_{gs} = Asinwt$), the Taylor

series expansion approximates the output signal as *(sin wt)*^{2} and *(sin wt)*^{3}, leading to an output frequency of 2*w* and 3*w*. Flexible CNT-FETs are observed to transform a 1 GHz RF signal to 2 GHz and 3 GHz signals (see Figure 7b) , thus, demonstrating a frequency multiplier operation as a frequency doubler and tripler. The flexible multiplication operation is characterized under different applied strains (see Figure 7c). When the strain is under 2%, the output power gain at 1 GHz, 2 GHz and 3 GHz frequency points are decreased as -0.5 dB, -0.55 dB and -0.6 dB, respectively, compared with the flat condition. From Figure 7c, it is observed that the frequency multiplier (doubler and tripler) can work normally under high level strain conditions (2%). However, when the strain increases to 3%, the output spectrum of the double (2 GHz) and triple (3 GHz) frequency signals are absent, indicating that the flexible CNT-FETs have lost the ability as a frequency multiplier.

The flexible CNT-FETs are also employed to design a microwave mixer to demonstrate its capacity for GHz frequency modulation (see Figure 7b). Here, a down-conversion mixer configuration is chosen because it is a critical component of RF receivers to demodulate an RF signals to a lower-frequency signal. Two microwave signals (f_{RF} =1 GHz and f_{LO} =1.8 GHz) are applied to the gate electrode of the flexible CNT-FETs via a power combiner. The drain electrode is connected to a microwave spectrum analyzer to test the output signal spectrum. As shown in Figure 7d , a clear output signal intensity for the intermediate frequency ($f_{IF} = f_{LO} - f_{RF} = 0.8$ GHz) tone appears when the CNT-FETs operate at $V_{gs} = -1$ V and $V_{ds} = -3$ V. It is deduced that the strain of 3% is the upper limit for mixer applications, beyond which limited performance is observed (shown in Supporting Information Figure S11). For the first time, this work demonstrates a GHz flexible microwave multiplier and mixer based on SWNTs flexible CNT-

FETs with a maximum operating strain of 2%. These results pave the way for future high-frequency nanotube flexible/wearable electronics with highly robust mechanical applications.

CONCLUSION

In summary, this work investigates a high-temperature annealing process and an Au nano-membrance transfer method for removing impurities in SWNTs and forming self-aligned ohmic contacts for high-performance flexible CNT-FETs, which can operate at GHz frequencies under high tensile strain. We also investigate the transistor's nonlinear effects and frequency conversion performance for GHz applications. Our results indicate that the fabricated flexible CNT-FETs have promising applications in GHz integrated circuits for wireless communication systems. This work offers a unique pathway for the adoption of nanotube materials for microwave applications in SWNTs based flexible/wearable electronics.

METHODS

Preparation of SWNT thin films on flexible PET substrates

High-purity semiconductor nanotube (99%) solution is purchased from Nano*Integris Inc. Toluene is used to dilute the CNT solution at a 10:1 volume ratio, followed by ultrasonic treatment for 10 min to obtain CNT suspension. A uniform SWNT thin film is fabricated using spin-coating method on a 500-μm thick Si wafer with a 500-nm SiO_2 layer (spin coated three times), followed by annealing at 900℃ under an Ar- and H_2-protected environment (the Ar and H_2 flow rate was 200 sccm:10 sccm) for 6 h. After depositing a 50-nm Au film on the surface of the SWNT thin film, a sandwich structure (Au/SWNTs/SiO_2/Si) is carefully floated on the surface of the HF solution to etch the SiO_2 layer. After fully etching the SiO_2 layer, the surface tension of water floats

the Au/SWNTs films on the surface of the HF solution and sinks the Si substrates. Finally, we directly transfer the Au/SWNTs films onto flexible PET substrates, followed by rinsing with DI water and baking at 100℃ for 12 h.

Fabrication of the flexible CNT-FETs

The fabrication process begins by spin casting a photoresist layer (AZ 7908, 3000 rmp/min, 30 s) as a protection layer for wet etching in KI: I_2 gold etchant solution, forming gold-covered isolation islands for the active areas. Standard lithographical resist (AZ 7908, 3000 rmp/min, 30 s) is used to define the gate channels. The Au film above the carbon nanotube in the gate channel is etched using KI: I_2 gold wet-etchant solution, followed by an 8-nm-thick Al_2O_3 layer deposition as gate dielectric and Ti/Au (50 nm/550 nm) layer as top gate electrodes. Finally, another photoresist (AZ 7908, 3000 rmp/min, 30s) layer is applied to deposit Ti/Au (50 nm/200 nm) layer to metallize the external source/drain test pads. A high-quality Al_2O_3 layer is obtained by water vapor ALD at a temperature of 100 ℃, which is compatible with low-temperature fabrication requirements for flexible electronics. An e-beam evaporator is employed for external source/drain metallization using a Ti/Au thickness of 50 nm/200 nm and gate electrode metallization with a Ti/Au thickness of 50 nm/550 nm.

Measurement and Analysis

The DC characteristics of the CNT-FETs are measured using semiconductor parameter analyzer. An Network Analyzer is used to measure the S-parameter of the CNT-FETs with a measurement setup calibrated to the G-S-G probe tips with a 150-μm pitch using a standard on-chip short-open-load-thru (SOLT) calibration kit. The S-parameters are obtained from the RF measurements, and

the "open-short de-embedded process" and the Spice equivalent small signal circuit model are analyzed using the Advanced Design System (ADS) software.

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Supporting Information Available

Potential and challenge of the carbon nanotube for flexible electronics, SEM images after annealing, fabrication details of the flexible CNT-FETs, Open-short calibration method, Extraction method of f_{max} and f_T, comparison of RF performance for different flexible nanomaterials, small signal equivalent circuit model, details for mobility estimation methods, cycle test of f_{max} (PDF).

The material is available free of charge *via* the Internet athttp://pubs.acs.org.

Author Contributions

Z. M firstly claimed the great potential and challenge of flexible RF electronics based on carbon nanotubes. Y. L, Y. X and Y. Y conceived the idea, directed the whole project. Y. L, Y. Y, S. H Y. W, Z. C and L. J finished the fabrication and measurement (DC and RF) of the flexible CNT-FETs. Y. L, Y.Y, L. J and S. H optimized the annealing parameters. Y. L, Y. W, Z, C, S, H and L, J contributed to the SEM and FIB images. Y. L, Y. Q.W, Y. G, Y. X, B. Y, Y. C and R. Xu finished

the RF measurement for the integrated circuits. Y. L, Y. W, Y. Q. W, Y. X and Y. L finished the original manuscript. Y. L, Y. X, S. L and Z. M finished the whole revision of the manuscript. Y. L and S. L finished the cover letter. All the authors contributed to the discussion of the data and results. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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Figure Captions

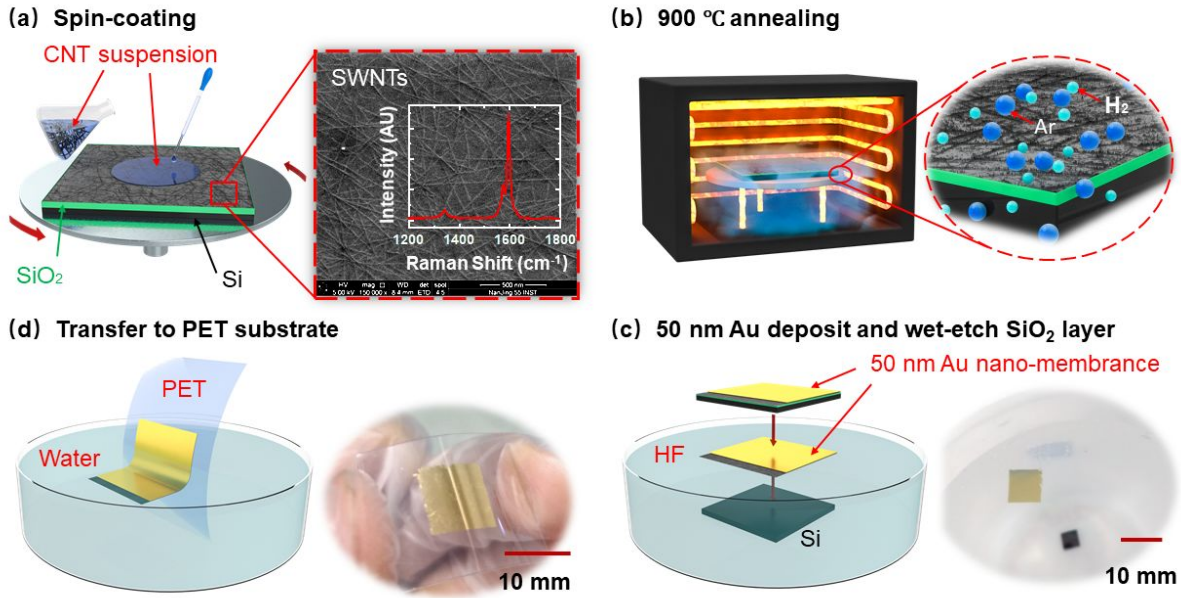

Figure 1. Schematic illustration (optical and scanning electron microscopy (SEM) images) of high-temperature annealed (900℃) SWNTs and their transfer onto flexible PET substrates. (a) Left: SWNTs are formed onto a 500 μm-thick Si wafer with a 500 nm-thick SiO_2 sacrificial layer by the method of spin-coating nanotubes suspension. Right: the SEM image exhibiting SWNTs thin films on the 500 nm-thick SiO_2 layer. Right inset: Raman spectroscopy of the semiconducting SWNTs after annealing at 900 ℃ for 6 hours. (b) A high-temperature (900℃) anneal is performed for SWNTs in argon (Ar) and hydrogen (H_2) ambient for 6 hours. (c) A 50 nm-thick Au film is deposited on SWNTs and yields a sandwich structure (Au/SWNTs/SiO_2/Si). This structure is then carefully floated on the HF surface to dissolve the sacrificial layer (SiO_2). (d)Transfer of the Au/SWNTs films onto flexible PET substrates is performed.

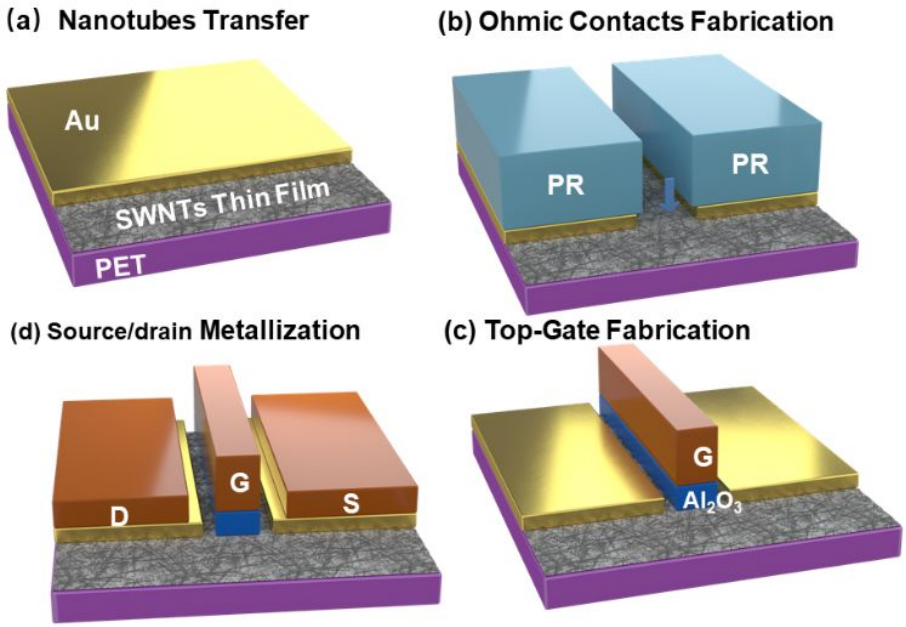

Figure 2. Schematic illustration of fabrication processes for RF CNT-FETs: (a) Transfer of SWNTs film onto a PET substrate; (b) standard photo-lithographical definition of the transistor's channel (channel length is 1.5 μm) areas and wet etching of the Au film to open channel regions. The wet etching process also aids in forming self-aligned ohmic contacts of the flexible CNT-FETs; (c) the deposition of a 8-nm-thick aluminum oxide layer by atomic layer deposition (ALD) as gate dielectric layer at 100°C and sputtering the gate metal stack of Ti/Au (30/550 nm); (d) the metal deposition of Ti/Au (30/200 nm) to thicken the source/drain pads.

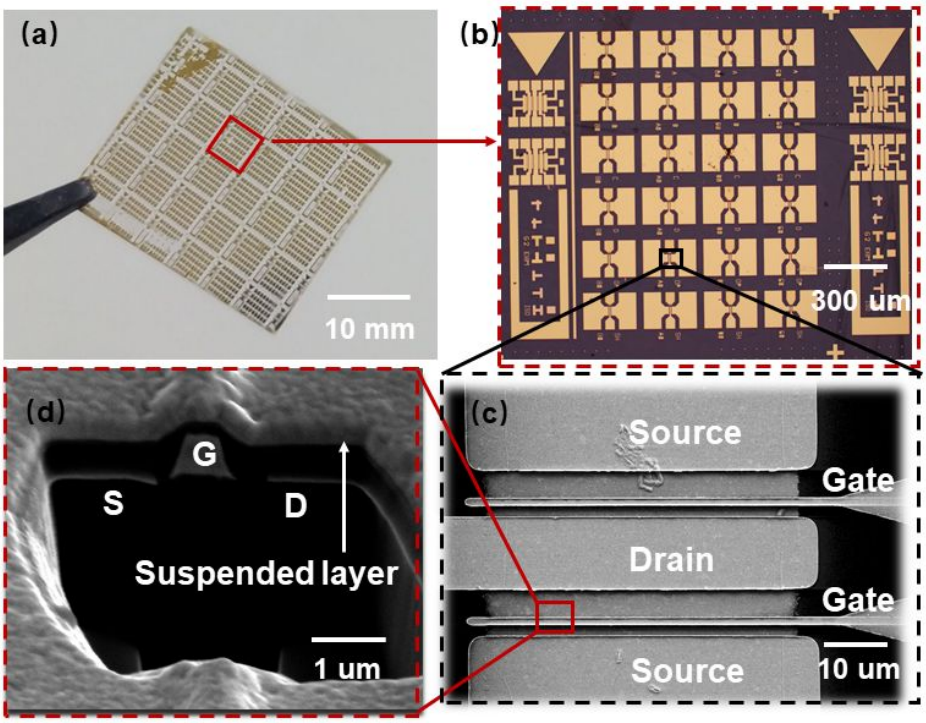

Figure 3. Optical, SEM and FIB images of the flexible CNT-FETs. (a) Optical microscope image of nanotubes FET array on a 20 mm × 20 mm bendable PET substrate. (b) Optical microscope image of 4 × 6 arrays CNT-FETs. (c) SEM of the active area of CNT-FETs. (d) FIB image of gate area. The channel length is about 1.5 μm, with a channel width of 2 × 60 μm. The suspending extra metal layer over gate and source/drain electrodes is deposited for FIB measurement due to the nonconductive properties of the plastic substrates.

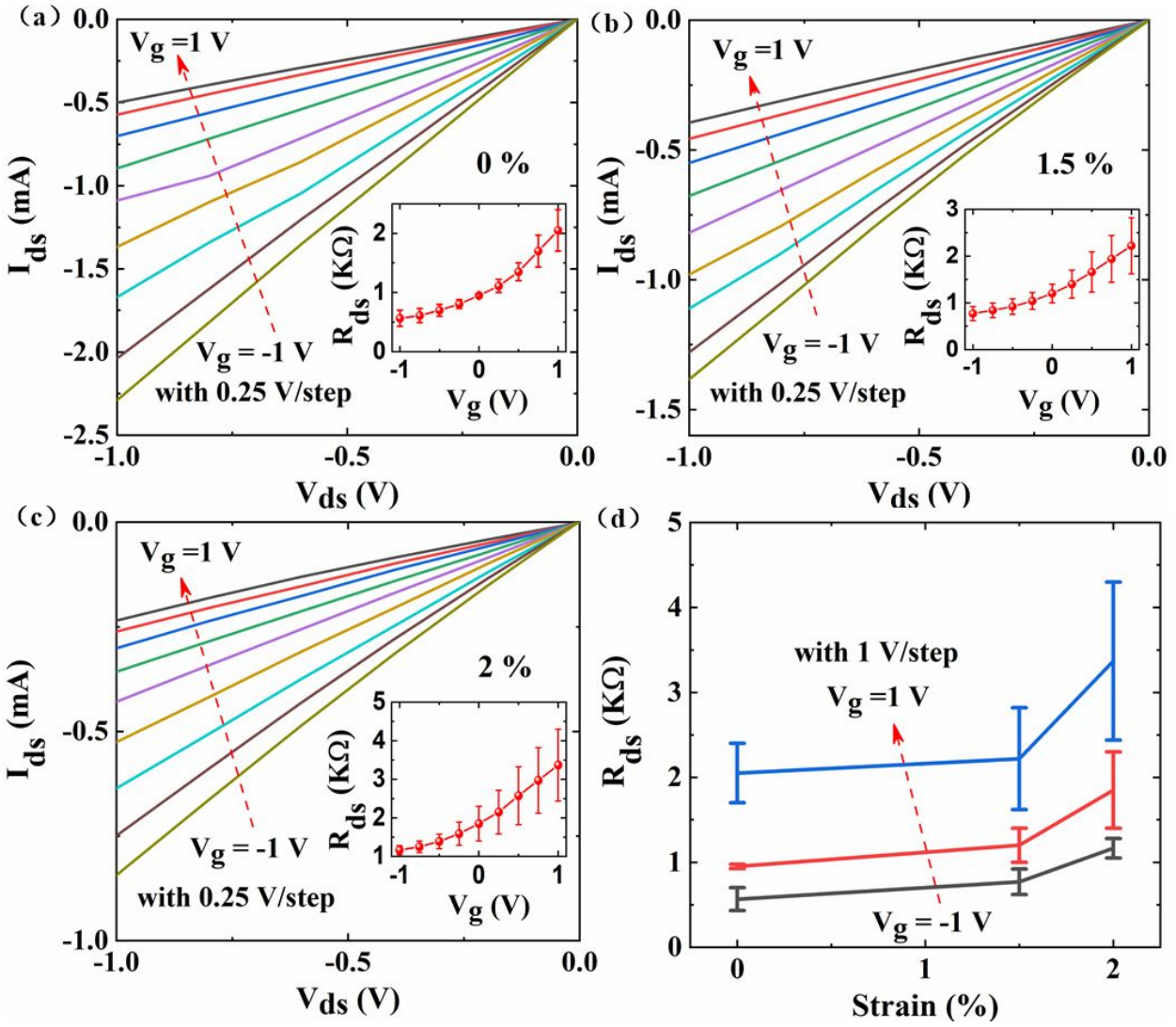

Figure 4. DC transfer and output characteristics of CNT-FETs on PET substrates under different tensile strain levels for V_{ds} ranging from −1 V to 0 V and V_g from −1 V (bottom) to 1 V (top), the V_g is varied in steps of 0. 25 V. (a) Measured I_{ds}-V_{ds} curves at a V_g from −1 V (bottom) to 1 V (top); the V_g is varied in steps of 0. 25 V. (b and c) I_{ds}-V_{ds} output curves at tensile strain of 1.5 % and 2 %, respectively. The inset represents transfer resistance (R_{ds}) curves with V_g sweeping from −1V to 1 V, showing the dependence of tensile strain. (d) Measured R_{ds} against different strain conditions (0%, 1.5% and 2%) at V_g of -1 V, 0V and 1 V.

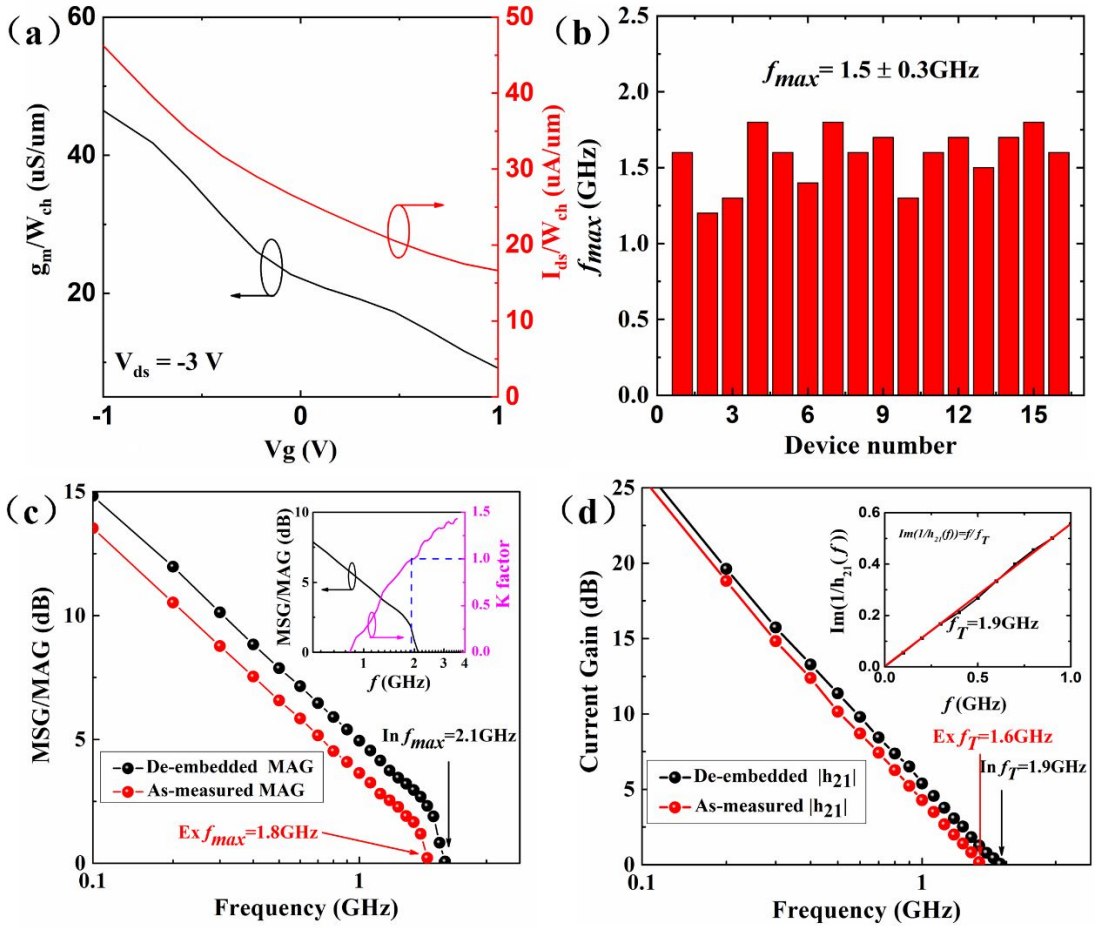

Figure 5. RF performance measurements for flexible CNT-FETs with a channel length (L_{ch}) of 1.5 μm and a channel width (W_{ch}) of 2 × 60 μm. (a) Transfer characteristic measurements for V_{gs} from −1 V to 1 V at a V_{ds} of −3 V. (b) Measured f_{max} statistics bars of sixteen flexible CNT-FETs with V_{ds}= -3V and V_{gs}=-1 V. The average and standard deviation are 1.5 and 0.3 GHz, respectively. (c) Available power gain (maximum stable gain (MSG)/MAG) shows that the f_{max} after pad embedding exceeds 2.1 GHz. The inset shows MSG/MAG to extract the pole transition point (k = 1). The pole transition point is measured at a frequency of 1.9 GHz. (d) Measured current gain $|h_{21}|$ vs frequency at V_{ds} = −3 V and V_{gs} = −1 V implies an extrinsic f_T of 1.9 GHz. Inset: Linear fitting by Gummel's extracted method, showing an extraction of the cutoff frequency almost identical to the plot of the main panel.

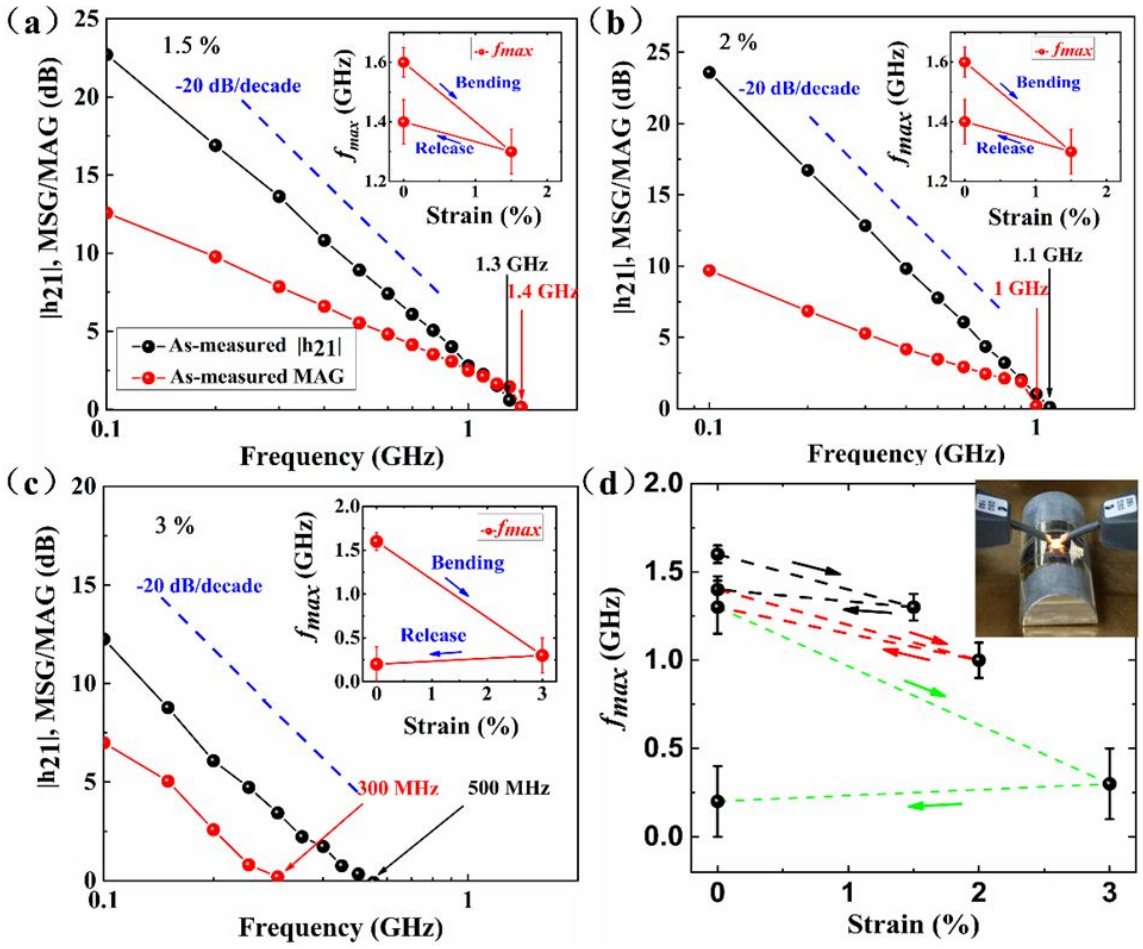

Figure 6. Current gain ($|h_{21}|$) and power gain (MSG/MAG) plotted against frequency for tensile strain of (a) ε=1.5%, (b) ε=2%, and (c) ε=3%, respectively. Inset images show a comparison of the RF performances under strain conditions and after the releasing strain. The blue dashed line is the theory slope (−20 dB/decade) that the MAG and h_{21} follow on a log-frequency scale. (d) Stepwise variation in f_{max} with the applied strain increase varying from 0% up to 3 %. The black dashed line shows the behavior of f_{max} as the strain changes from 0 to 1,5% and then from 1.5% to 0%, wherein the arrows denote the change, While the red and green dashed lines represent the f_{max}'s dependence on applying and releasing a strain of 2% and 3%, respectively, and then the strain is released to 0%. Inset image shows optical photographs of the measurement layout under strain conditions. The devices comprise of a L_{ch} of 1.5 μm and W_{ch} 2 × 60 μm.

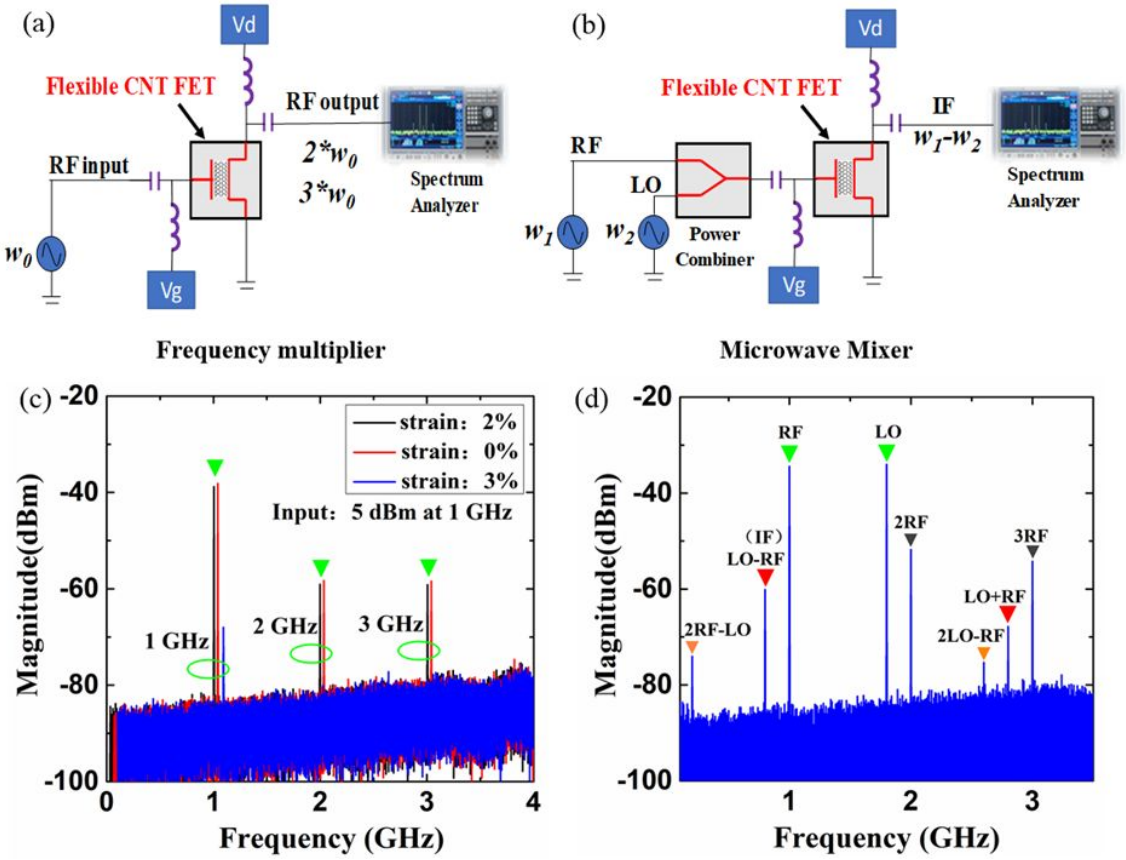

Figure 7. Schematic and measured output spectrums of the GHz-frequency multiplier and mixer. (a) Schematic of the measurement setup for frequency multiplier using a microwave spectrum analyzer. (b) Measured schematic of a mixer with RF and LO input signals. (c) Measured output spectrum of the CNT-FETs based frequency multiplier with 1 GHz input signal (power level of 5 dBm) at different strain levels (0%, 2%, and 3%). The frequency doubler and frequency tripler work normally at strain level of 0% and 2%, but fail their function when the applied strain increase to 3%. (d) Measured output of CNT-FETs based mixer with the following parameters: RF=1 GHz and LO=1.8 GHz at equal power of 5 dBm, where the modulation product of 800 MHz (IF) clearly appears.

Table 1: Comparison of high-frequency performance for flexible RF thin-film transistors comprising of different nanomaterial systems (including SWNTs, graphene, BP, MoS_2, and Ⅲ-Ⅴ nanowires).

Reference	Material	Substrate	L_{ch} (μm)	Ext f_T (GHz)	Ext f_{max} (GHz)	f_{max}×L_{ch} (GHz×μm)
This work	Solution SWNT networks	PET	1.5	1.8	2.1	3.15
21	DEP SWNT array	PET	0.8	0.4	—	—
22	Solution SWNT networks	PI	4	0.17	0.12	0.48
34	InAs nanowire network	PI	1.5	1.08	1.8	2.7
35	Solution graphene film	PI	0.26	2.2	0.55	0.143
28	CVD graphene	PET	0.3	31	28	8.4
36	Exfo. BP	PI	0.5	7	10.3	5.15
37	CVD MoS_2	PI	1	2.7	2.1	2.1

*DEP: dielectrophoresis; PI: polymide; Exfo: mechanically exfoliated; CVD: chemical vapor deposition

Graphical TOC Entry