

On the Use of Scalable NanoISFET Arrays of Silicon with Highly Reproducible Sensor Performance for Biosensor Applications

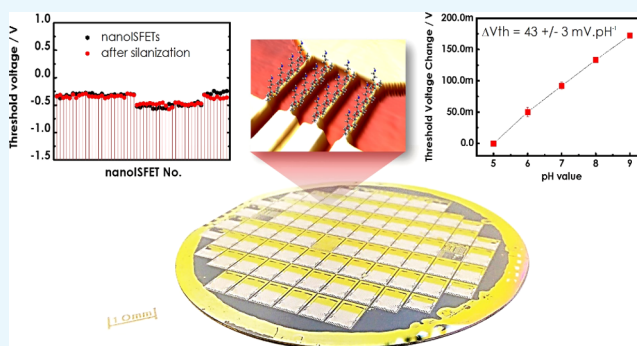
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Supporting Information

ABSTRACT: As a prerequisite to the development of real label-free bioassay applications, a high-throughput top-down nanofabrication process is carried out with a combination of nanoimprint lithography, anisotropic wet-etching, and photolithography methods realizing nanoISFET arrays that are then analyzed for identical sensor characteristics. Here, a newly designed array-based sensor chip exhibits 32 high aspect ratio silicon nanowires (SiNWs) laid out in parallel with 8 unit groups that are connected to a very highly doped, Π -shaped common source and individual drain contacts. Intricately designed contact lines exert equal feed-line resistances and capacitances to homogenize the sensor response as well as to minimize parasitic transport effects and to render easy integration of a fluidic layer on top. The scalable nanofabrication process as outlined in this article casts out a total of 2496 nanowires (NWs) on a 4 inch p-type silicon-on-insulator (SOI) wafer, yielding 78 sensor chips based on nanoISFET arrays. The sensor platform exhibiting high-performance transistor characteristics in buffer solutions is thoroughly characterized using state-of-the-art surface and electrical measurement techniques. Deploying a pH sensor in liquid buffers after high-quality gas-phase silanization, nanoISFET arrays demonstrate typical pH sensor behavior with sensitivity as high as $43 \pm 3 \text{ mV} \cdot \text{pH}^{-1}$ and a device-to-device variation of 7% at the wafer scale. Demonstration of a high-density sensor platform with uniform characteristics such as nanoISFET arrays of silicon (Si) in a routine and refined nanofabrication process may serve as an ideal solution deployable for real assay-based applications.



INTRODUCTION

Nanoscale ion-sensitive field-effect transistors (nanoISFETs) as the centerpiece of modern electrochemical sensing platforms attract a relentless pursuit to develop new label-free assays for real biomedical applications and other similar fields.^{1–7} In recent years, the discovery of low-dimensional material systems and their integration onto electrical sensor platforms using novel nanofabrication methods have dramatically improved the capabilities of nanoISFETs, such as improved sensitivity, selectivity, and ability for analyte multiplexing.^{6–15} Prototype studies in recent years have focused on the use of semiconductor nanowires (semi-NWs), carbon nanotubes (CNTs), graphene-based materials (GBMs), and two-dimensional (2D) semiconductor materials as high surface-to-volume ratio electrical transducers with versatile surface characteristics for realizing ultrafast and label-free detection of biomolecules.^{16–25} On the basis of current trends in the development of nanoISFET-based sensor platforms and bioassays, it is suggested that label-free detection approaches may soon provide breakthroughs in the field of in vitro diagnostics (IVD) and compete against otherwise tedious and expensive

bioanalytical methods involving preamplification of analytes, for example, polymerase chain reactions (PCRs) and enzyme-linked immunosorbent assays (ELISAs).^{3,26–30}

Although label-free nanoISFET platforms mentioned above outdo current bioanalytical tools in terms of sensor performance, the deployment of candidate nanomaterials for mainstream applications largely depends on the possibility of scaling up their respective nanofabrication processes. Despite increasing knowledge in molecular biology techniques and the discovery of new biomarkers, lack of cost-effective and near-industry fabrication for many of the high-performance nanoISFET platforms hampers the development pace of novel bioassay technologies.³¹ Optimization of new bioassay techniques before going through clinical testing and final implementation in the respective biomedical fields critically requires limiting the number of specific clinical tests during the developmental phases to reduce the overall costs.^{32–34} Here,

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the silicon (Si)-based technology offers a unique opportunity for well-established nanofabrication methods and control over material properties and their impressive track-record toward the development of novel biosensor concepts.^{2,35–38} More recently, Si-based biosensor platforms have been deployed for bioassay optimization in a variety of near-clinical studies using nucleic acids, antibodies, and enzymes as analyte biomarkers.^{28,39–42} Additionally, Si-based ISFETs have been a workhorse for studying live cell signals using different signal acquisition approaches and are identified as a potential platform for drug-discovery and diagnostic applications.^{22,43} With this immense know-how in biosensor development, Si-based nanoISFETs are more than ever facilitating the development of new, label-free electronic assays, their optimization, and final implementation for real diagnostic applications.

In the context of high-throughput use and efficient clinical analysis of new bioassays, here we demonstrate a new approach for the high-density fabrication of nanoISFET arrays of Si in a top-down approach and analyze uniformity of their sensor characteristics over the wafer scale. A mixed nanofabrication process involving nanoimprint lithography, anisotropic wet-chemical etching, and photolithography processes is worked out on a 4 inch silicon-on-insulator (SOI) wafer where a total of 2496 enhanced-mode nanoISFET are fabricated and distributed over 78 individual sensor chips. Sensor chips are specially designed in a dip-chip configuration where 32 individually addressable high aspect ratio nanoISFETs are connected to a Π -shaped common source and individual drain contact lines. The source and drain contact lines are intricately designed and highly doped to exert equal capacitance and resistance for each channel and to minimize the parasitic transport effects. Thorough characterization of nanoISFET arrays reveals highly uniform surface and transport characteristics with minimal device-to-device variations in sensor properties. Randomly chosen and deployed as a pH sensor in liquids, nanoISFETs showed pH sensitivity as high as 43 ± 3 mV·pH⁻¹ with a device-to-device variation of around 7%. Ascribing the highly uniform sensor characteristics of our nanoISFET arrays to an optimized top-down fabrication approach reinforced by special design and adequate property considerations for contact lines, we demonstrate a very reliable and versatile platform to analyze complex label-free bioassays.

RESULTS AND DISCUSSION

The realization of a nanoISFET array-based sensor platform began with the consideration of the need for a high-throughput and multiplex sensor platform with multiple readout possibility from identical sensor sites on a chip. At first, we designed a nanoimprint lithography mold for our nanoISFET arrays-based sensor chips using a graphics program (Clewin) to be realized on a 5 inch Si wafer with a 200 nm SiO₂ layer on top using e-beam lithography and a dry-etching process (Institute of Microelectronics Stuttgart, Germany). Figure 1A shows the layout of an individual sensor chip measuring 10×7 mm² where 32 high aspect ratio SiNWs are positioned in an array form in the group of 4, making 8 unit groups, that is, 32 individually addressable sensor sites. An individual unit group is shown on the right in the zoomed-in view taken from the layout where 15 micron long SiNWs are separated by a 5 micron distance. The NW units are separated by 250 microns so as to later on facilitate selective deposition of biomolecules for bioassay applications using microspotting techniques.⁴⁴ Sensor signals from the four nanoISFETs of a unit could then

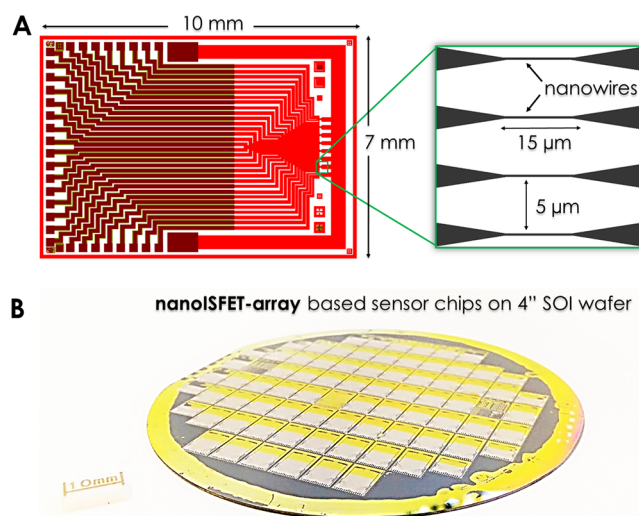


Figure 1. Scalable fabrication of sensor chips with nanoISFET arrays based on Si. (A) Layout of a sensor chip showing a Π -shaped source contact and individual drain contact lines. The nanoISFET arrays are grouped into eight subunits where one subunit is shown in the inset. Individual NWs measure 15 micron in length and are separated by 5 microns. (B) Photograph showing a 4 inch SOI wafer with nanoISFET-array sensor chips.

be averaged to improve the reliability of the assay readout. The NWs are connected to a common Π -shaped source electrode in a special configuration to allow the positioning of nanoISFET arrays closer to the edge of the sensor chip, which is advantageous for the deployment of chips in a “dip-chip” configuration, as well as to facilitate easy integration of a fluidic platform on top. To facilitate parallel readout and multiplexing capabilities, each nanoISFET is connected to individual drain electrodes. To avoid sensor characteristic variances coming from parasitic capacitances and contact-line resistances, drain electrodes are intricately designed to keep the total capacitance and inline resistance values identical for all 32 nanoISFET arrays. The sheet resistance and capacitance of the contact lines were calculated using a theoretical model for charge-carrier doping in Si (see Supporting Information). Figure 1B shows a photograph of a 4 inch SOI wafer with 78 sensor chips coming out at the end of the fabrication process. The nanofabrication process for the realization of nanoISFET arrays is outlined in Figure 2. 8 inch SOI wafers (SOI-Prime-8-880/1450Å) with an 88 nm Si layer and 145 nm SiO₂ layer were procured from Soitec, France. The SOI wafers were then laser-cut into 4 inch wafers at WINFAB in Catholic University Louvain and cleaned following a standard protocol using the Radio Corporation of America (RCA) procedure. Ellipsometry measurements were carried out in our lab on these wafers, which confirmed the top Si layer thickness of 87 nm and a buried oxide (BOX) thickness of 145 ± 6 nm (see Supporting Information). The wafers are of prime quality grown using low boron (p-type) doping, resistivity values ranging from 8 to 22 Ω ·cm, and a crystal orientation of $\langle 100 \rangle$. Before processing the wafers, the top Si layer was thinned down using thermal oxidation (hard mask growth) to reach a thickness of 67 nm with an oxide thickness of 45 nm, which was confirmed by ellipsometry measurements (see Supporting Information). A thinned-down SOI wafer as shown in Figure 2i is spin-coated with nanoimprint thermal resist MR9030 (purchased from Micro Resist Technology GmbH) to get a 700 nm thick layer and baked for 2 min at 100

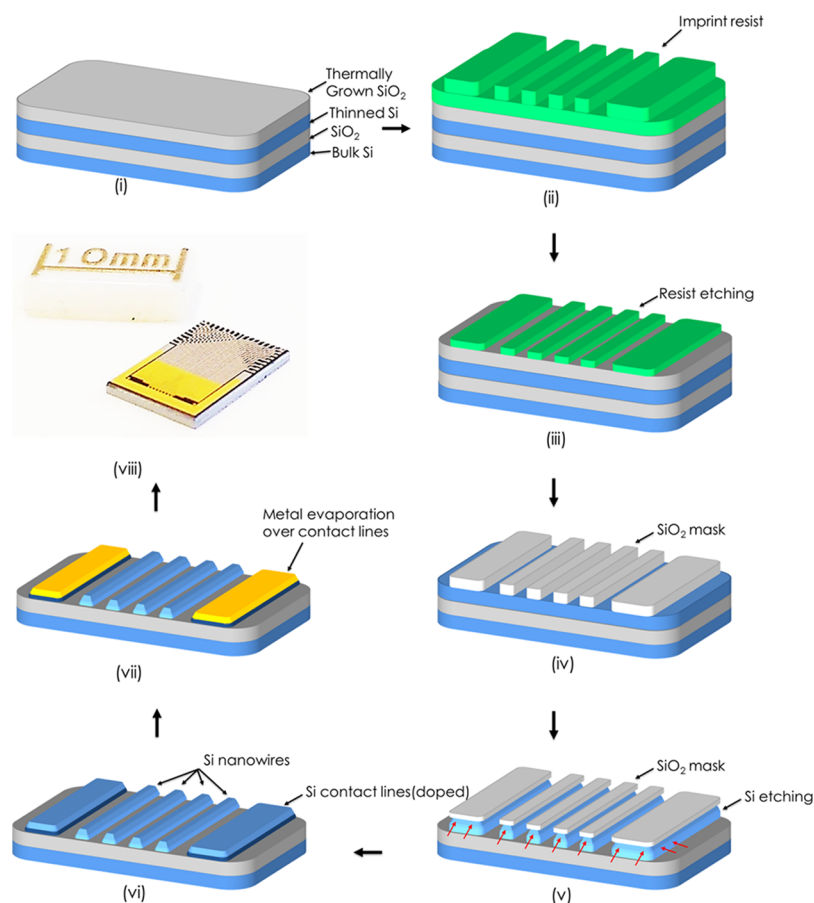


Figure 2. Schematics showing the process flow for the fabrication of the nanoISFET arrays. (i) Prime quality SOI wafers are thinned down by growing SiO_2 in a dry oxidation process, (ii) thermoresist-coated SOI wafer after the nanoimprint process, (iii) RIE of the imprinted thermoresist, (iv) successive dry-etching process for the removal of the thermoresist and down to the structure of the SiO_2 layer as well, (v) wet anisotropic etching of the Si layer casting out trapezoidal cross-sections for SiNW arrays, (vi) SiNW and contact-line structures casted out from the Si layer after the boron ion implantation of contact lines (one photolithography step used for passivation), (vii) photolithography step for the evaporation of Al/Ti/Au over the implanted Si contact lines using another photolithography process and liftoff, and (viii) resulting 7×10 mm dip-chip layouts of the 32 channel nanoISFET arrays.

$^{\circ}\text{C}$ to remove any moisture. The imprint on this thermal resist was carried out by pressing the stamp against the resist layer at 95°C for 900 s at 50 bar pressure and demolding at 40°C . A mirror pattern now imprinted into the resist layer (Figure 2ii) is then used as a mask for structuring the 45 nm thick SiO_2 layer underneath in the next step. The imprinted residual layer of the thermal resist is now dry-etched using a reactive-ion etching (RIE) process in 20 sccm O_2 at 100 W and 2 Pa for 240 s (Figure 2iii). The etching process is continued to transfer the pattern onto the SiO_2 layer underneath (RIE is carried out in 30 sccm CHF_3 at 200 W and 3 Pa for 100 s) (Figure 2iv). The thus patterned SiO_2 layer is now used as a hard mask for structuring the underlying Si layer, where an anisotropic wet-etching is carried out by the use of tetramethylammoniumhydroxide (TMAH) solution (Figure 2v).^{45,46} With the culmination of this anisotropic wet-etching, the SiNWs and contact-line patterns on the mold are finally transferred onto the thin Si top layer of the SOI wafer and result in parallel production of high aspect ratio SiNW-arrays. For Si layer etching, first the wafers are cleaned with fresh piranha solution for 10 min followed by dipping them into 1% hydrogen fluoride (HF) solution for 120 s to remove the left over hard mask. Etching is carried out by dipping the wafers into 25% TMAH solution at 90°C for 60 s. This series of etching processes transfers the mold design onto

the top Si layer of the SOI wafers. The structured top Si layer of SOI wafers cast out into NW arrays exhibits semiconductor characteristics with resistivity around $8\text{--}22\ \Omega\cdot\text{cm}$. In the next step, the source and drain contact lines patterned in the top Si layer connecting NWs to external contacts were p-doped (boron) using an ion-implantation process (Ion Beam Services Peynier, France). Doping of contact lines helps to reduce the serial resistances while retaining the high carrier mobility of the Si nanowire (SiNW) channels.⁴⁶ The doping process is controlled by the ion-implantation energy, dose, and thickness of the passivation layer on the SiNW region. The ion implantation energy defines the projection range in the Si layer calculable from the Stopping and Range of Ions in Matter (SRIM) program based on the quantum mechanical treatment of the ion-atom collision.⁴⁷ An ion projection of 40 nm was targeted to have only the top Si layer implanted, where an implantation energy of 10 keV was calculated with an implantation dose of 10^{15} atoms/ cm^2 with irradiation at a 7° tilt (see Supporting Information). To carry out implantation of contact lines, a photolithography step was performed to passivate the SiNW arrays by a photoresist layer as protection from ion implantation. After implantation, ions were activated by a high-temperature annealing step at 850°C for 30 min under a nitrogen atmosphere followed by thermal dry oxide

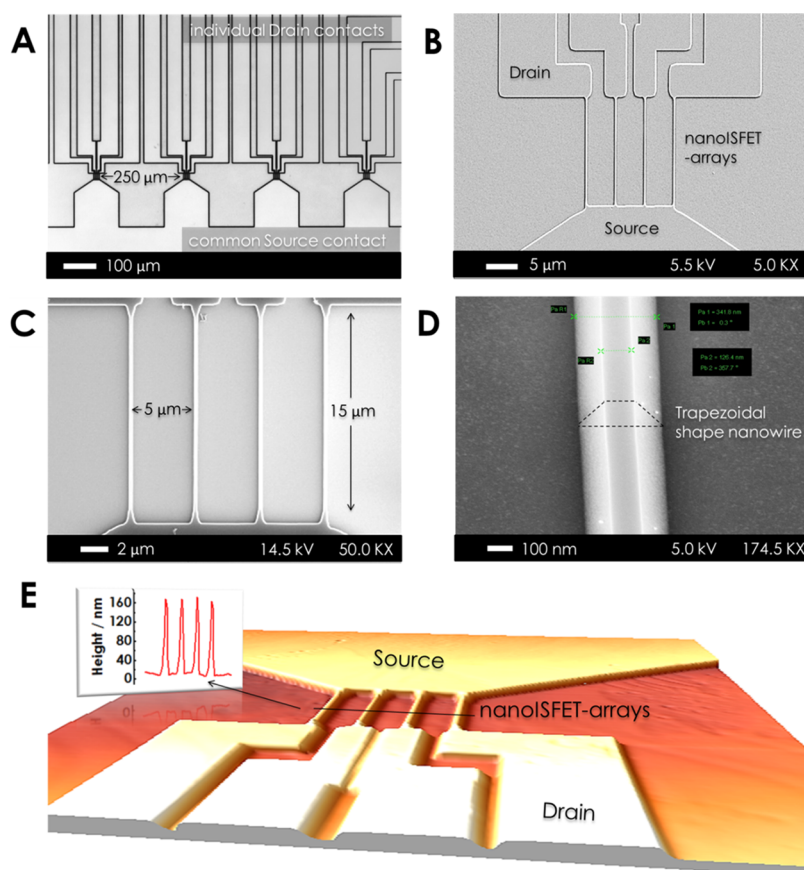


Figure 3. Structural characterization of nanoscale ISFET arrays. (A) Zoomed-out optical microscopy image of the sensor chip showing four out of the eight ISFET-array units. ISFET arrays are connected to a common source and individual drain contact lines. (B) SEM image of a nanoISFET-array unit showing four high aspect ratio NWs connected to a common source and intricately designed individual drain contact lines. (C) Zoomed-in SEM scan showing detailed structural characteristics of the array. The identical NWs measure 15 micron in length with a spacing of 5 micron in between. (D) Further zoomed-in SEM scan of an individual NW showing trapezoidal cross-section and smooth edges after the wet-chemical etching process. (E) Detailed three-dimensional view of a nanoISFET-array unit on a sensor chip characterized using AFM. The height of the individual NWs measures around 160 nm as shown in the inset.

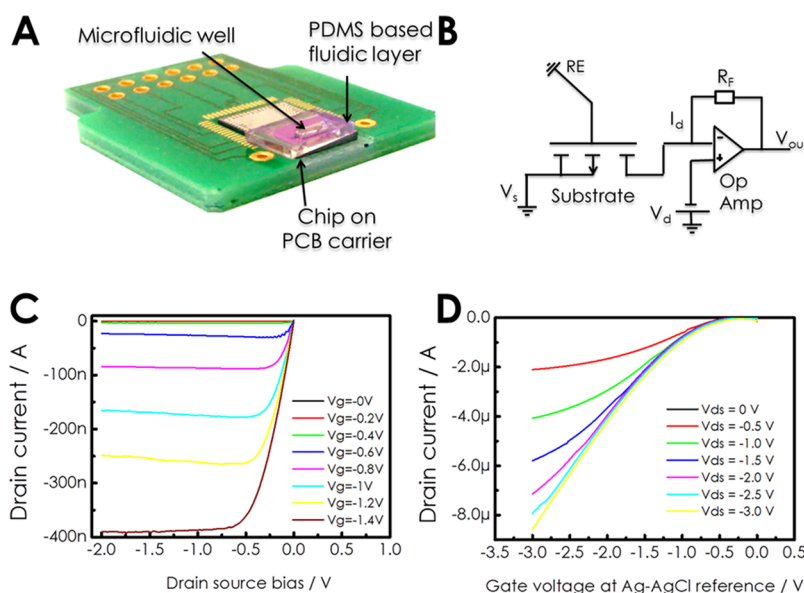


Figure 4. Field-effect characteristics of an exemplary nanoISFET in a liquid gate configuration. (A) Setup used for the measurement of electrochemical field-effect characteristics where the sensor chip is mounted on a PCB carrier and wire bonded to external contacts. A fluidic layer based on PDMS is placed on top of the chip for easy handling of liquid buffers. (B) Circuit diagram of the measurement setup, (C) current–voltage output characteristics of a typical p-type nanoISFET, and (D) typical transfer characteristics of a nanoISFET in buffer solution.

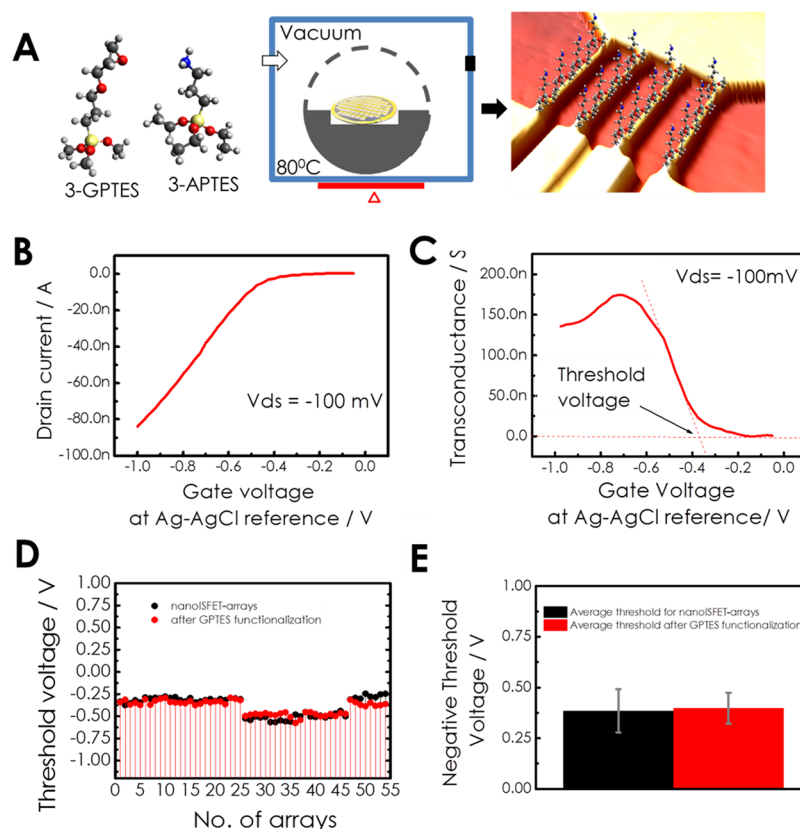


Figure 5. Sensor characteristics of the nanoISFET arrays of Si. (A) Surface functionalization of nanoISFET arrays is carried out by using candidate silanes such as APTES and GPTES in a gas-phase silanization technique. (B) Field-effect curve for a typical nanoISFET in a liquid taken at a drain–source bias of -100 mV, (C) transconductance plot of the nanoISFET and the calculation of the threshold voltage, (D) mapping threshold response of nanoISFET arrays measured at pH 7 before and after the silanization process, and (E) histogram showing variations in the threshold voltage at pH 7 before and after the silanization process.

(SiO₂) layer generation on the Si surface at 810 °C for 45 min, which measured around 8 nm and also worked as a gate dielectric (Figure 2vi). Finally, a UV photolithography step covered the contact lines and contact pad areas with a metal layer composed of Al (150 nm), Ti (20 nm), and Au (200 nm) as inferred from Figure 2vii. After the metal evaporation, wafers were annealed in a vacuum at 350 °C for 10 min to ensure good electrical contacts. The deposition of metals on the contact line ensures low resistance for charge carriers flowing out of the nanoISFET arrays.⁴⁶

Structural characterization of nanoISFET arrays is shown in Figure 3. Figure 3A shows an optical image from a portion of the sensor chip after carrying out the nanoimprint process where four units are shown with four identical SiNWs each. Figure 3B shows a scanning electron microscopy (SEM) image of a unit performed on a Zeiss Supra 40 microscope where SiNWs are seen connected to a common source and individual drain contact lines. Also from Figure 3A,B, it is quite clear that after optimization of the nanoimprint process results in homogeneous filling of the thermoresist in all of the micro- and nano-features of the mold. Figure 3C shows a zoomed-in SEM image of four Si high aspect ratio SiNW arrays coming out of our nanoimprint lithography process. The NW arrays are 15 micron long and lie parallel to each other with a 5 micron spacing in between. The NW surfaces appear very smooth and identical in structural details, which is further highlighted in a higher-resolution SEM scan shown in Figure 3D. The SEM image details the finer structural details of the SiNWs resulting

after the wet-etching. TMAH etches Si anisotropically because of a lower etching rate at the $\langle 111 \rangle$ plane than that of other planes, therefore resulting in a trapezoidal cross-section.⁴⁵ This provides a precisely controllable mechanism and results in smooth surfaces with low defects. From the detailed SEM and AFM (Veeco Dimensions 3100) characterization (Figure 3E), individual SiNWs are measured in width at 126 nm on the top side and 340 nm at the base. As inferred from the AFM scan image, SiNWs have a total height of 160 nm, which is known from our process because of the etching of BOX. Therefore, the SiNW arrays are elevated from the BOX floor leading to an almost “wrapped around gate” configuration.⁴⁸

Figure 4 describes the characterization of nanoISFET arrays of Si realized in this newly optimized nanofabrication process for liquid sensing applications using the electrochemical gate configuration. Figure 4A shows a nanoISFET arrays-based sensor chip mounted on a specially designed printed circuit board (PCB) where the source and drain contacts on the chip are wire bonded to connect to the electrical measurement system. The chip was assembled with a fluidic reservoir of polydimethylsiloxane (PDMS Sylgard 184) to facilitate the handling of liquid solutions during the measurements. All measurements were performed on a semiconductor parameter measurement setup (Keithley 4200 SCS). Figure 4B shows the circuit diagram of the measurement setup for ISFET arrays in a three-electrode configuration. An electrochemical electrode made of silver/silver chloride (Ag/AgCl) was used as a reference electrode (450 μ m Dri-Ref from WPI Europe). All of

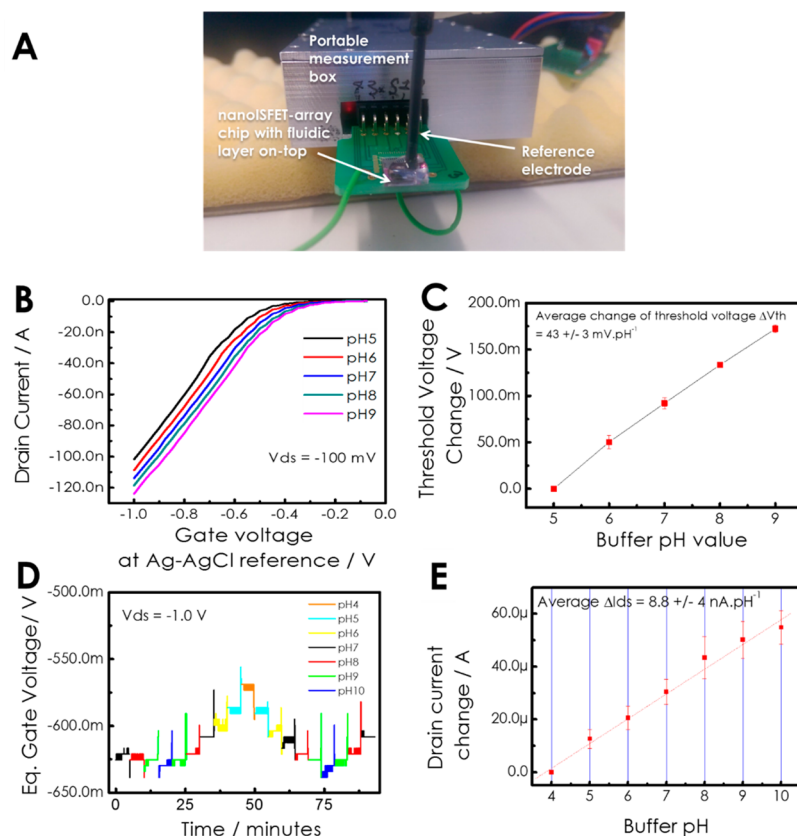


Figure 6. Deployment of nanoISFET arrays as a miniaturized hand-held sensor platform. (A) Photograph of the miniaturized measurement setup for real-time pH sensing using nanoISFET arrays of Si. (B,C) pH dependent field-effect characteristics of the nanoISFET arrays show a linear pH response with sensitivity as high as 43 ± 3 mV/pH. (D,E) Real-time pH sensor recording from nanoISFET arrays using buffers with pH values ranging from pH 4 to 10.

the electrical characteristic measurements were carried out in a 10 mM phosphate buffer (PB) at pH 7. Figure 4C shows the output characteristics of an individual nanoISFET as shown in Figure 3. Here, the source–drain bias (V_{ds}) was swept between 0 to -2.0 V, and the bias at the Ag/AgCl reference electrode (V_g) was applied from 0.0 to -1.4 V in steps of -0.2 V. For an enhancement-mode field-effect device, there is no drain current (I_{ds}) passing at $V_g = 0$ V, which is below the threshold voltage (V_{th}). When the bias voltage applied at the reference electrode is greater than the threshold voltage ($V_g > V_{th}$), I_{ds} increases and shows linear behavior at low drain–source bias values. The linear behavior of I_{ds} at low bias is explained by $I_{ds} \propto (V_g - V_{th}) V_{ds}$, while at larger drain–source bias, a saturation condition is achieved as explained by $I_{ds} \propto (V_g - V_{th})^2$. Figure 4D shows the exemplary transfer characteristics of a typical SiNW at a linear scale where V_g is varied from 0 to -3 V and V_{ds} voltage is varied from 0.0 to -3.0 V in steps of -0.5 V. The SiNW arrays presented p-type enhancement-mode transistor characteristics. The p-type enhancement-mode output characteristics of the nanoISFET arrays result from the charge-carrier depletion in the SiNW structure compared to the highly implanted drain and source contacts. Unlike in standard metal oxide semiconductor field-effect transistor (MOSFET) structures, the hole carriers in the SOI structure cannot be recruited from the substrate. Here, the carrier injection and enhancement of charge-carrier density are occurring from the source and drain contacts into the fully depleted SiNWs.

After the basic characterization for the operational range of the SiNW arrays, we deployed them as pH sensors to ascertain

the sensor characteristics, reproducibility, and random variation in their sensor characteristics. SiNW array chips were chosen randomly and surface-modified with pH-sensitive molecules by employing a gas-phase silanization method.⁴⁹ The chips were cleaned in a piranha solution (1:3 ratio of H_2O_2 and H_2SO_4) for 10 min at 60 °C to have a high density of hydroxyl groups on the NW surface before being subjected to the silanization process. The silanization process was carried out inside of a vacuum atmosphere where 200 μ L of 3-glycidyloxypropyltrimethoxysilane (GPTES) or 3-aminopropyltriethoxysilane (APTES) was injected into a container tube connected to a vacuum chamber where SiNW arrays were placed in an oxygen-free environment as shown in the schematic of Figure 5A. The vacuum chamber was then heated up to 80 °C, and the silanization process was performed for 2 h and 30 min. After silanization, chips were cleaned with deionized (DI) water to remove excess silane. In this surface functionalization process, silane molecules assembled themselves on the SiNWs by forming a bond with the hydroxyl groups present on the NW surface. The gas-phase silanization methods are better suited for realizing highly homogeneous self-assemblies of molecular layers over large surface areas against other protocols.⁴⁹ It is known that upon functionalization of oxide surfaces with aminosilanes, the pH-sensing mechanism based on protonation and deprotonation of functional groups moved from being exclusively based on hydroxyl groups to a combination of amino ($-NH_2$) and hydroxyl ($-OH$) groups present at the surface, representing a variety of surface densities and dissociation constants at a particular pH. At low pH values,

the amino group was protonated to NH_3^+ , and at high pH values, SiOH was deprotonated to $-\text{SiO}^-$, leading to an almost linear relation of surface charge with pH.

Field-effect characteristics of silanized nanoISFETs in buffer at pH 7 are shown in Figure 5B where -100 mV bias (V_{ds}) was applied, whereas V_{g} was swept from 0 to -1 V. To ascertain device-to-device variations in sensor characteristics, we took the V_{th} of the nanoISFETs at pH 7 as a reference. V_{th} is extracted from the output characteristics for all of the devices measured. The threshold voltage of nanoISFETs is calculated by implementing a transconductance (g_{m}) extrapolation method where the first derivative of I_{d} ($\text{d}I_{\text{d}}/\text{d}V_{\text{g}}$) is plotted against V_{g} as shown in Figure 5C.⁵⁰ (see Supporting Information) From the g_{m} values in buffer solutions, the field-effect mobility (μ) of the ISFET arrays is calculated at around $1.97 \text{ cm}^2/\text{V}\cdot\text{s}$. The threshold response (V_{th} values) of 54 randomly chosen nanoISFET arrays is shown in Figure 5D before and after GPTES silanization. Upon silanization of SiO_2 surfaces with GPTES, the total negative surface charge on the nanoISFETs is expected to decrease because of the replacement of the hydroxyl groups with glycidoxo groups, requiring a higher negative gate voltage to “switch on” the device and therefore an increase in the threshold voltage.⁵¹ Interestingly, some of the nanoISFET arrays exhibit an aberration as shown in Figure 5D for channels from no. 26 to 45, the reasons for which are discussed in detail in the Supporting Information, which potentially arises from the variations in effective channel lengths. On average, as shown in Figure 5E, V_{th} values of nanoISFET arrays before and after the silanization process were calculated at 384 ± 106 and 395 ± 76 mV, respectively, accounting for device-to-device variations of 27.6 and 17.2%. The overall increase in the threshold voltage upon GPTES functionalization of the nanoISFETs stays in agreement with the theoretical interpretations.⁵¹ In addition to slight variations in sensor characteristics coming from the mask-alignment process as discussed in detail in the Supporting Information, inherent factors of the nanofabrication such as the dopant concentration variation during the implantation step, variation in the gate oxide thickness, and fixed charges over the wafer may play a crucial role in determining the homogeneity of sensor characteristics.^{52,53}

Furthermore, nanoISFET arrays are deployed for the measurement of output characteristics at a drain–source bias of -100 mV and sweeping the voltage at the reference electrode from 0 to -1.0 V while changing the buffer solutions from pH values 5 to 9 to evaluate (Figure 6B) the pH sensor response and variation as a basis for future bioassay applications. On the basis of these measurements, the pH sensitivity of the nanoISFET arrays is plotted in Figure 6C as the change (ΔV_{th}) in buffer solutions at different pH values. A linear pH response with small error bars is observed, showing highly reproducible sensor characteristics with pH sensitivity as high as 43 ± 3 mV/pH accounting for only a 7% device-to-device variation. The pH sensitivity of the nanoISFET arrays as presented here is comparable to that of the other NW-based platforms reported in the literature.^{54–57} It is documented that ISFETs with bare SiO_2 surfaces exhibit a sensor response on the order of 34 mV/pH , which may increase up to 45 mV/pH with the modification of the oxide surface with functional molecules such as APTES.⁵⁶ High-throughput clinical analysis of novel bioassays is critical to the development of label-free IVD and other related applications where a closely knit sensor response from a high-density sensor platform such as the

nanoISFET arrays of Si realized in this work may provide an appropriate platform. Although high-performance and precise sensor characteristics were achieved, we took a closer look at the different factors that may be playing a role in the tiny variations of the pH response from nanoISFET arrays, which will be investigated and rectified in further work (see Supporting Information). Going a step further toward the application of such sensor platforms for point-of-care (PoC) applications, we connected our nanoISFET arrays to a portable hand-held readout system for field-effect-based biosensor arrays which was recently developed in our group.⁵⁶ Figure 6A shows the photograph of this portable measurement setup where the sensor chip is mounted on a PCB and connected to the four-channel miniaturized readout system built around a 32 bit PIC microcontroller and equipped with a user-friendly readout software designed in LabView communicating with the hardware to record and display the electrical measurements on a computer screen or any other device. The sensor chip is also equipped with a fluidic layer to facilitate pH sensor measurements in real time for longer periods. Figure 6D shows an exemplary real-time sensor measurement while going through multiple cycles of changing buffer solutions with pH values ranging from 4 to 10. In these measurements, nanoISFET arrays were operated at maximum sensitivity, that is, applying V_{g} corresponding to maximum transconductance values at a given bias V_{d} (-1 V). For the measurement shown in Figure 6D, -1.5 V V_{g} was applied and I_{d} was recorded. The I_{d} values were converted to equivalent gate voltage values and plotted against time while changing the buffer solutions. The nanoISFET arrays were generally operated for more than an hour and exhibited a stable sensor response over multiple cycles. An average pH response from 5 nanoISFET arrays in the form of an average equivalent gate voltage change (ΔV_{gs}) is plotted in Figure 6E, which is demonstrating the portability of our nanoISFET array sensor system. This platform can now be applied for future point of care applications.

MATERIALS AND METHODS

The nanoimprint lithography mold was purchased from the Institute for Microelectronics Stuttgart, Germany. The optical masks used for all photolithography processes were purchased from Delta Masks Enschede, the Netherlands. SOI wafers were purchased from Soitec, France, and were cut into 100 mm wafers at the Catholic University of Louvain, Belgium. Thermoresists, photoresists, and other chemicals such as H_2SO_4 , 1% HF, and 25% TMAH were purchased from MicroChemicals GmbH, Germany. APTES and GPTES were purchased from Sigma Aldrich, Germany. The nanoimprint lithography, photolithography processes, and other measurements were carried out at the University of Applied Sciences Kaiserslautern, Campus Zweibruecken. A Keithley 4200 semiconductor parameter analyzer from Tektronix, GmbH was used for electrical measurements in a three-electrode configuration. Ag/AgCl reference electrodes (DR1REF-450) were bought from World Precision Instruments. For pH measurements 10 mM PB was prepared by mixing disodium hydrogenphosphate (Na_2HPO_4) and sodium hypophosphate (NaH_2PO_4) salts in DI water to obtain solutions of different pH values.

CONCLUSIONS

A new near-industry nanofabrication process is optimized for the realization of nanoISFET arrays of Si for assay-based applications. Sensor chips with 32 individually addressable nanoISFET are fabricated by combining nanoimprint lithography, photolithography, and anisotropic wet-chemical etching methods. Special configurations of nanoISFET arrays with highly doped contact lines ensure identical sensor characteristics and result in the assembly of a sensor platform with reliable, high-performance, and near-identical sensor characteristics. Deploying as pH sensors, nanoISFET arrays of Si demonstrate exemplary sensor characteristics with pH sensitivity as high as 43 ± 3 mV/pH and a device-to-device variation of 7%. Finally coupled with a hand-held readout system, the sensor platform demonstrates the potential for real-time sensor measurement capabilities in liquids. Wafer scale realization of a high-density sensor platform as demonstrated in this article may in the near future serve as a workhorse for carrying out high-throughput and multiplex analysis of clinical tests and play a key role in the development of label-free assays and PoC solutions paving a path toward real diagnostics applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsomega.6b00014.

Further details about the thickness measurement method of the Si and SiO₂ thin film, the method to calculate the capacitance and resistance values of the contact lines, field-effect mobility value, ion-implantation measurements, the limitations of the nanolithography processes and its effect on the device performance, issues such as mask alignment during the lithography process, use of open microfluidic reservoirs, and placement of the reference electrode and their effect on the measurements (PDF)

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Author Contributions

The manuscript was prepared by D.R. under the supervision of V.P. The fabrication process was carried out by D.R. with contributions from A.M., V.P., D.R., V.P., and S.I. discussed the results included in the article.

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Notes

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