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To cite this article before publication: Ganesh Jayakumar *et al* 2019 *Nanotechnology* in press <https://doi.org/10.1088/1361-6528/ab0469>

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Pixel-based biosensor for enhanced control: Silicon nanowires monolithically integrated with field-effect transistors in fully depleted silicon on insulator technology

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Abstract

Silicon nanowires (SiNWs) are widely used technology for sensing applications. Complementary metal-oxide-semiconductor (CMOS) integration of SiNWs advances lab-on-chip (LOC) technology and offers opportunities for read-out circuit integration, selective and multiplexed detection. In this work, we propose novel scalable pixel-based biosensors exploiting the integration of SiNWs with CMOS in fully-depleted silicon-on-insulator (FDSOI) technology. A detailed description of the wafer-scale fabrication of SiNW pixel using the CMOS compatible sidewall-transfer-lithography (STL) as an alternative to widely investigated time inefficient e-beam lithography is presented. Each 60 nm wide SiNWs sensor is monolithically connected to a control transistor and novel on-chip fluid-gate forming an individual pixel that can be operated in two modes: biasing transistor frontgate (V_G) or substrate backgate (V_{BG}). We also present the first electrical results of single N and P-type SiNW pixels. In frontgate mode, N and P-type SiNW pixels exhibit $SS \approx 70 - 80$ mV/dec and $I_{on}/I_{off} \approx 10^5$. The N-type and P-type pixel has an average threshold voltage, V_{th} of -1.7 V and 0.85 V respectively. In the backgate mode, N and P-type SiNW pixels exhibit $SS \approx 100 - 150$ mV/dec and $I_{on}/I_{off} \approx 10^6$. The N and P-type pixel has an average V_{th} of 5 V and -2.5 V respectively. Further, the influence of the backgate and frontgate voltage on the switching characteristics of the SiNW pixels is also studied. In the frontgate mode, the V_{th} of the SiNW pixel can be tuned at 0.2 V for 1 V change in V_{BG} for N-type or at -0.2 V for -1 V change in V_{BG} for P-type respectively. In the backgate mode, it is found that for stable operation of the pixels, the V_G of the N and P-type transistor must be in the range 0.5 to 2.5 V and 0 V to -2.5 V respectively.

Keywords: silicon nanowire pixel; silicon nanowire biosensor; lab-on-chip; SiNW CMOS integration; selective multiplexed detection; SiNW frontgate mode; SiNW backgate mode

1. Introduction

Over the past 40 years, lab-on-chip (LOC) technology has been the center of attention of research due to its great potential for portable, low cost and label-free early detection of diseases [1]. Highly sensitive label-free detection can be achieved using micro cantilevers and surface plasmon resonance mass spectrometry [2]–[6]. However, the complex nature of detection and signal acquisition limit their usage [2]. On the other hand, silicon nanowires (SiNW) configured as field effect transistor (FET) offer high sensitive and label free detection [7]–[12]. The electrical readout in SiNWs is based on detection of charges on its surface passivated with a dielectric material such as SiO₂ (Figure 1). Initially, the current flowing through the SiNW is measured without any bio molecule addition and its threshold voltage is noted (V_{th1}). Later, the surface of the SiNW is functionalized with the receptors and target of interest. Then, the current flowing through the SiNW is re-measured. The bio molecule addition causes a change in the surface charge density (Q_{hybrid}) resulting in the shift of the threshold voltage of the SiNW (V_{th2}). By noting the difference in the threshold voltages ($\Delta V_{th} = V_{th2} - V_{th1}$) before and after biomolecule addition, the amount of charge (N_{hybrid}) resulting from the target molecule of interest can be estimated using equation 1 [13].

$$N_{hybrid} = \frac{Q_{hybrid}}{q} = -\Delta V_{th} \frac{\epsilon_0 \epsilon_r}{q t_{ox}} \quad (\text{Equation 1})$$

where ϵ_0 is the vacuum permittivity ($\epsilon_0 = 8.85 \times 10^{-14} \text{ F.cm}^{-1}$), ϵ_r the relative permittivity of the gate dielectric ($\epsilon_r = 3.9$ for SiO₂) and t_{ox} its thickness and q is the charge of electron ($q = -1.6 \times 10^{-19} \text{ C}$).

SiNW-FET's have been well-established to manufacture standalone DNA, protein, microRNA and strepavidin sensors [8], [10], [12], [14]–[20]. Furthermore, the excellent structural properties of SiNW such as 1D structure (small size), high surface to volume ratio and a dimension comparable to the target of interest make them an ideal building block in LOC sensors for bio detection [8], [10], [12], [14]–[20]. Yet, as seen from table 1 not much work has been done in the area of complementary metal oxide semiconductor (CMOS) integration of SiNW to fabricate a complete LOC. Advantages such as read out circuit integration, selective and multiplexed real-time detection could be gained by integrating SiNW with CMOS transistors [21], [22]. However, the device architecture necessary for exploiting the SiNW integration with CMOS is rarely addressed. Thus, the aim of this work is to address the integration of SiNW with CMOS circuits.

In our previous work, we proposed one such scalable sequentially read-out scheme to integrate SiNW with CMOS where each SiNW is connected to a control transistor and an on-chip fluid gate forming a SiNW pixel (Figure 2) [21], [22]. 'N x N' matrix of such pixels can be addressed using N-bit vertical and horizontal shift register circuits respectively [23]. In the design, the transistor is configured as a switch for row and column selection. The output current of the pixel array

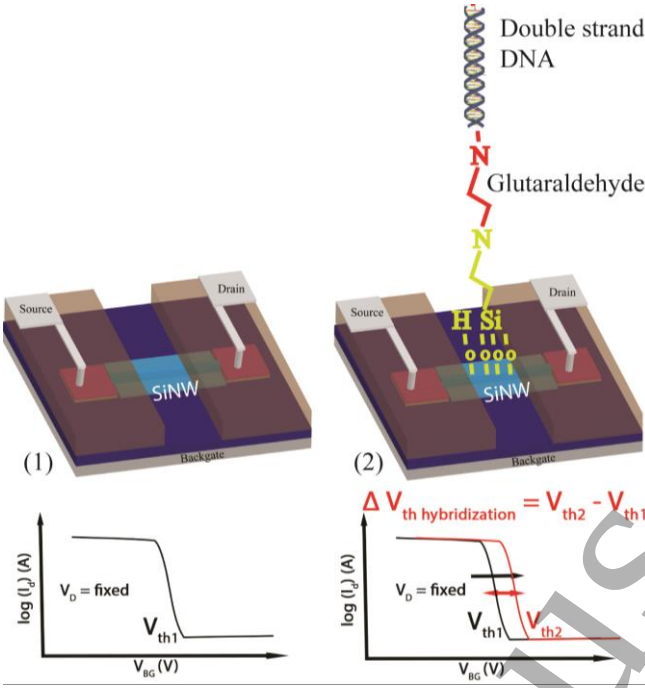


Figure 1. A schematic depicting the working principle of a SiNW sensor. (1) In the first step, the threshold voltage (V_{th1}) of the SiNW sensor is measured before bio molecule addition. (2) In the next step, the surface of the SiNW is functionalized with the target molecule such as double strand DNA where it undergoes hybridization process. Hence, the surface charge on the SiNW changes resulting in threshold voltage (V_{th2}). The added charge on the surface can be estimated by noting the change in the threshold voltage ($V_{th2} - V_{th1}$).

Table 1: A literature review of some of the most important works employing SiNW sensor for the detection of pH or bio targets. The distinction is made on account of fabrication method (top- down (TD) versus bottom-up (BU)), substrate type (Bulk Si versus silicon-on-insulator (SOI)) and type of sensor. Further, the application and CMOS integration feature is also taken into consideration.

Reference	Fabrication method, substrate, device type	CMOS integration	Application
Na Lu et al. [8]	TD, SOI, SiNW	No	miRNAs
Agarwal et al. [10]	TD, SOI, SiNW	No	ss-DNA
Gao et al. [12]	TD, SOI, SiNW	No	ss-DNA
Kong et al. [14]	TD, SOI, SiNW	No	Cardiac troponin I (cTnI)
Nguyen et al. [15]	BU, Bulk, SiNN-FET	No	DNA
Zhang et al. [16]	TD, SOI, SiNW	No	miRNAs
Pui et al. [17]	TD, SOI, SiNW	No	pro-inflammatory cytokines
Chen et al. [18]	TD, SOI, SiNW	No	ss-DNA
Knopfmacher et al. [19]	TD, SOI, SiNW	No	pH
Tarasov et al. [20]	TD, SOI, SiNW	No	pH, ions

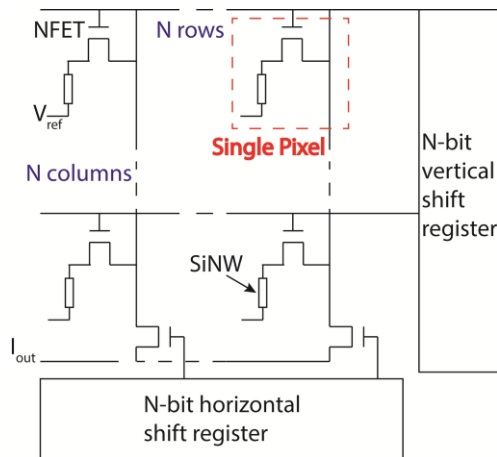


Figure 2. Circuit diagram of a SiNW pixel-based LOC. Each SiNW is connected to an on-chip fluid gate and a control transistor forming a SiNW pixel [13]. ‘N x N’ matrix of such pixels can be addressed using N-bit vertical and horizontal shift register circuits respectively.

could further be monolithically connected to circuits such as amplifiers for signal amplitude magnification, band pass filters for reducing the noise or allowing only a certain range of the signal and other read-out circuits such as a trans-impedance amplifier to convert current to voltage output. Jieun et al have explored one such option [24]. Yet, in their work only a single SiNW biosensor is connected with an amplifier to enhance the current response. Furthermore, their approach of mix-match manufacturing process used in the hybrid sensor fabrication increases the cost and time of production. Our preliminary aim was not to achieve signal amplification but to explore the selective and multiplexed detection scheme. Therefore, individual SiNW sensors of critical dimensions 60 nm were connected with N and P-type CMOS transistors (length (L) = 1 μm and width (W) = 4 μm) to fully exploit the monolithic integration of SiNW with CMOS transistors. In such a scheme, the individual SiNWs can be turned ON or OFF by using the transistor as a switch.

In order to monolithically integrate SiNWs with CMOS circuits, the manufacturing scheme utilized for the realization of the SiNW pixel must be CMOS compatible. In literature, there are two well-established methods to manufacture SiNW – 1) Bottom-up (BU) 2) Top-down (TD) [2], [9], [15], [19], [25]–[27]. In the bottom-up method, the SiNW are grown on a Si bulk wafer using the vapor-liquid-solid (VLS) technique [18], [28]. In the BU method, molecular precursors such as silane, SiH_4 and diborane B_2H_6 for p-type (and phosphine, PH_3 for n-type) along with gold nanoparticle as a catalyst are used to grow the SiNWs [29]. However, the limitation of this technique is that the grown SiNWs are randomly placed and appear as tangled meshes. As a result they require special techniques such as dielectrophoresis and application of an electric field to align the SiNWs [9], [15], [26], [27], [30]. Further, it is quite challenging to transfer the grown SiNWs on to a CMOS chip as it can lead to manual errors, contaminants and poor contact formation due to breakage of SiNWs [30]. On the other hand, the TD method relies on the well-established CMOS industry standard lithography and etching techniques to form the SiNWs [10], [18], [19], [21], [22], [28], [30]. Since the TD method is directly compatible with CMOS technology and materials, it is straightforward to integrate SiNWs with CMOS circuits using this approach [21], [30], [31].

Thus, in this article, we present a detailed description of the wafer scale fabrication of SiNW pixel using the fully CMOS compatible top-down sidewall-transfer-lithography (STL) as an alternative to widely investigated time inefficient e-beam lithography [21], [31]. Then, we show the first electrical results of the pixel design for both N and P-type SiNW pixels. The SiNW pixels can be operated in two different modes - the frontgate as well as backgate mode. In the frontgate mode, the pixel is turned ON or OFF by applying a frontgate voltage to the N and P-type transistor while the backgate bias is fixed. In the backgate mode, the pixel is turned ON or OFF by applying a backgate voltage to the substrate while the frontgate bias of the N and P-type transistor is fixed. Both these schemes validate the concept of accessing individual SiNW pixel modules in a matrix of sensors. Hence, this work expands the capability of SiNW by integration with CMOS. Furthermore, the pixel-based design also opens new frontiers for manufacturing SiNW based LOC sensors that has provision for multiplexed detection of different biomarkers.

2. Methods and Materials

2.1 Fabrication

The SiNW pixel sensors were fabricated on a boron doped ($1 \times 10^{15} \text{ cm}^{-3}$) 4" (100 mm) silicon on insulator (SOI) wafer using the STL process [21], [23], [31]–[33]. The detailed steps in the fabrication of the SiNW pixel sensor are shown in Figure A1 of the supplementary section.

Table 2 shows the N and P-type pixels that were fabricated in this work. The dimensions of the corresponding control transistor and nanowire module in the respective pixel is also shown. Single N-type SiNW of $W = 60 \text{ nm}$ and $L = 1, 2$ and $6 \text{ }\mu\text{m}$ is connected to N-type control transistor of $L = 1 \text{ }\mu\text{m}$ and $W = 4 \text{ }\mu\text{m}$ respectively. Single P-type SiNW of $W = 60 \text{ nm}$ and $L = 1, 2$ and $6 \text{ }\mu\text{m}$ is connected to P-type control transistor of $L = 1 \text{ }\mu\text{m}$ and $W = 4 \text{ }\mu\text{m}$ respectively.

Table 2: Geometrical characteristics of the six SiNW pixel devices studied in this work. The thickness of the SiNW sensors is 20 nm. In a N-type pixel, a N-type transistor of $L = 1 \text{ }\mu\text{m}$ and $W = 4 \text{ }\mu\text{m}$ is connected to a N-type SiNW sensor of $L = 1, 2$ and $6 \text{ }\mu\text{m}$ and $W = 60 \text{ nm}$. Similarly, in the P-type pixel, a P-type transistor of $L = 1 \text{ }\mu\text{m}$ and $W = 4 \text{ }\mu\text{m}$ is connected to a P-type SiNW sensor of $L = 1, 2$ and $6 \text{ }\mu\text{m}$ and $W = 60 \text{ nm}$.

Type of pixel	Type of transistor	Transistor dimensions		Type of SiNW	SiNW dimensions	
		L (μm)	W (μm)		L (μm)	W (nm)
N	N	1	4	N	1	60
					2	
					6	
					1	

P	P	1	4	P	2	60
					6	

2.2 Electrical characterization

The setup shown in Figure A1(K-L) was used for the electrical evaluation of the SiNW pixel sensors prior to functionalization. Electrical DC measurements were performed on wafer scale by using a Cascade 12000 semi-automatic wafer prober. The wafer prober was externally connected to a Keithley 4200-SCS parameter analyzer. All measurements presented in this work were performed at room temperature ($T = 300$ K) on 4" wafer. Wafer scale measurements were performed to demonstrate the high throughput and reproducibility of the STL fabrication process for SiNW pixel manufacturing. Further, as it is important to preserve the integrity of the SiNW sensors before and after opening access to the test site, the electrical evaluation of the SiNW pixel sensors was performed at two steps [23], [32]. Figure A1(K) shows the electrical setup used to characterize the SiNW before opening access to the test site. In this setup, a thick 400 nm PECVD passivation oxide is still present on top of the SiNW. Figure A1(L) shows the electrical setup used to characterize the SiNW after opening access to the test site. In this setup, the thick 400 nm PECVD passivation oxide is removed using RIE as discussed in previous section 2.1 and access to the SiNW test site is provided.

In the SiNW pixel, the source terminal of the transistor is connected to the column selection line while the drain terminal of the transistor is connected to the SiNW. The SiNW pixel can be operated in two modes – the backgate mode and frontgate mode (Figure 3). In the backgate mode, the gate of the MOSFET is biased at a fixed frontgate voltage while the SiNW is turned ON or OFF by sweeping the backgate voltage (Figure 3(B)). In the backgate mode, to turn ON the SiNW pixel, sufficient frontgate voltage needs to be applied such that the MOSFET is first turned ON (Figure 3(B)). In the frontgate mode, the MOSFET is turned ON or OFF by sweeping the frontgate while the SiNW is biased at a fixed backgate voltage (Figure 3(C)). In the frontgate mode, to turn ON the SiNW pixel, sufficient backgate voltage needs to be applied such that the SiNW is first turned ON. The SiNW behaves like a resistor in the frontgate mode as it is turned ON/OFF using the backgate voltage (Figure 3(C)).

In the backgate mode, an initial bias voltage of -0.1 V for PMOS (or 0.1 V for NMOS) was applied to the drain terminal (V_D) while the source terminal (V_S) was connected to the ground. Then, a bias voltage of 0 V was applied to the gate of the control transistor (both NMOS and PMOS), while the backgate was swept from -15 V to +15 V. In the frontgate mode, the gate of the transistor (V_G) is swept from -2.5 to +2.5 V and an initial bias voltage of -0.1 V for PMOS (or 0.1 V for NMOS) was applied to the drain terminal (V_D) while the source terminal (V_S) was connected to the ground. The SiNW was turned ON by applying a constant bias voltage to the backgate (V_{BG}). In both modes of operation, the fluid gate terminal

(V_{FG}) was left open and not connected as these measurements were performed prior to bio functionalization. However, in the liquid environment the fluid gate can be configured to monitor changes in the pH. For example, a change in pH of the electrolyte environment from pH₁ to pH₂, would give rise to output current I_{D1} and I_{D2} respectively. In order to track the changes in the pH, the fluid gate potential can be changed such that the two currents I_{D1} and I_{D2} are equal. According to the Nernstian equation [7][19-20],

$$\Delta V_{FG} = 2.303 \frac{k_B T}{q} \Delta pH \text{ (Equation 2) (when } I_{D1} = I_{D2} \text{)}$$

where ΔV_{FG} is the change in the fluid gate voltage, k_B is the Boltzman constant, q is the electron charge and ΔpH is the change in the pH (from pH₁ to pH₂).

Thus, by noting the changes in the fluid gate potential, it is possible to estimate the change in the pH value in the liquid environment.

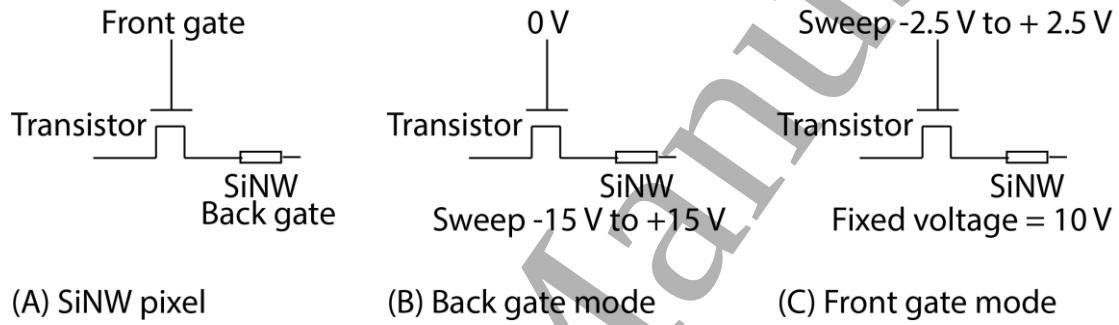


Figure 3. (A) The test setup for electrical evaluation of the SiNW pixel sensors in (B) backgate mode where frontgate of the control transistor is fixed at 0 V while the backgate of the SiNW is swept from -15 V to 15 V (C) frontgate mode where the transistor frontgate is swept from -2.5 V to 2.5 V and SiNW is biased at fixed voltage where it is always ON (-10 V for P-type SiNW and 10 V for N-type SiNW).

The subthreshold slope (SS) and threshold voltage (V_{TH}) of the SiNW pixels and transistors were noted from the transfer characteristics. The linear extrapolation method was employed to extract the V_{TH} of the SiNW pixels and the transistors. In the subsequent sections, the wafer scale electrical characteristics of the SiNW pixel sensors are presented.

3. Results and discussion

3.1 I_D - V_G transfer characteristics of N and P-type transistor

Figure 4(A) shows the I_D - V_G transfer characteristics (at $V_{BG} = 0$ V) of P-type and N-type control transistors manufactured on SOI wafer. The NMOS and PMOS transistors have a SS of 60 – 65 mV/dec. The extracted V_{TH} for NMOS is in the range from -0.3 to 0.3 V while the PMOS transistor has V_{TH} in the range of -0.9 to -1.1 V. In the frontgate mode, when a backgate voltage is applied to switch ON the SiNW in the pixel module, the control transistor is also impacted. Thus, the

influence of V_{BG} on individual N and P-type transistors was also studied in this work to determine the stable region of operation in backgate mode. During the electrical measurements of NMOS transistor, the V_G was swept from -2.5 to 2.5 V while keeping the V_S at 0 V, V_D at 0.1 V and stepping V_{BG} (-15, -10, -5, 0, 5, 10, 15, 20, 25 and 50 V). Similarly, in the case of the PMOS transistor, the V_G was swept from -2.5 to 2.5 V while keeping the V_S at 0 V, V_D at -0.1 V and stepping V_{BG} (-50, -25, -20, -15, -10, -5, 0, 5, 10, 15 V). Figure 4(B) and figure 4(C) shows the I_D - V_G transfer characteristics of a single PMOS and NMOS device manufactured on SOI wafer at different V_{BG} .

In the case of PMOS (Figure 4(B)), the blue color I_D - V_G curve is at $V_{BG} = 0$ V. The positive V_{BG} values cause the I_D - V_G transfer characteristics to shift to the left side (green color) of the I_D - V_G curve at $V_{BG} = 0$ V as the back interface is in accumulation. The V_{TH} decreases by ≈ 20 -25 mV for 1 V change in V_{BG} . The SS is only slightly influenced. Whereas the negative V_{BG} values cause the I_D - V_G transfer characteristics to shift more towards the right side (orange color) of the I_D - V_G curve at $V_{BG} = 0$ V as the Si/BOX interface approaches inversion. At $-50 \text{ V} \leq V_{BG} \leq -25 \text{ V}$, the frontgate control over the channel is gradually lost causing the increase in SS. As a result, at V_{BG} values $> -25 \text{ V}$, the transistor can no longer be turned OFF. For $-25 \text{ V} \leq V_{BG} \leq -5 \text{ V}$, the V_{TH} linearly depends on V_{BG} and changes by ≈ 100 mV for -1 V change in V_{BG} .

Likewise, in the case of NMOS (Figure 4(C)), the blue color I_D - V_G curve is at $V_{BG} = 0$ V. The negative V_{BG} values cause the I_D - V_G transfer characteristics to shift to the right side (orange color) of the black curve as the back interface is in accumulation. The V_{TH} linearly increases by ≈ 20 -25 mV for 1 V change in V_{BG} . The SS is only slightly influenced. Whereas, the positive V_{BG} values cause the I_D - V_G transfer characteristics to shift more towards the left side (green color) of the I_D - V_G curve at $V_{BG} = 0$ V as the Si/BOX interface approaches inversion. At $50 \text{ V} \leq V_{BG} \leq 15 \text{ V}$, the frontgate control over the channel is gradually lost causing the increase in SS. As a result, at V_{BG} values $> 25 \text{ V}$, the transistor can no longer be turned OFF. For $15 \text{ V} \leq V_{BG} \leq 5 \text{ V}$, the V_{TH} linearly depends on V_{BG} and changes by ≈ 100 mV for 1 V change in V_{BG} .

Thus, it is established that for stable operation of the SiNW pixel it is essential to restrict the V_{BG} in the range -10 V to 10 V.

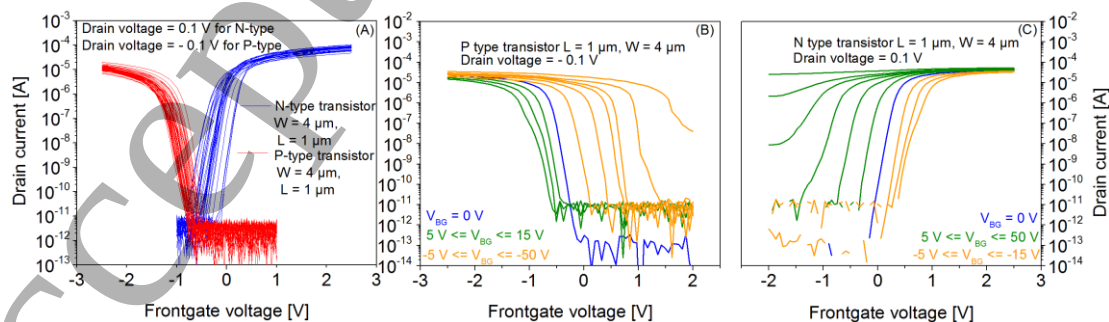


Figure 4. (A) The wafer scale I_D - V_G transfer characteristics of standalone NMOS and PMOS transistors. The backgate voltage is set to 0 V during the measurements. I_D - V_G transfer characteristics of a single (B) P-type (C) N-type control FET at different V_{BG} values. It is established that application of V_{BG} ($>20 \text{ V}$ for N-type and $> -25 \text{ V}$ for P-type) pushes the

devices into strong inversion regime of operation, which impacts the V_{TH} and SS of the devices.

3.2 Influence of backgate voltage on CMOS circuits

In the final LOC device architecture, the CMOS read circuits are also connected at the input and output of the SiNW (figure 2). Thus, the V_{BG} applied to switch ON the SiNW pixel sensor can influence the output characteristics of the connected CMOS circuits as they share the same backgate. To study the influence of V_{BG} on the CMOS circuits, an inverter circuit was electrically characterized at different substrate bias voltages ($-20 \text{ V} \leq V_{BG} \leq 20 \text{ V}$, in steps of 5 V). The V_{DD} of the inverter was set to 2 V ; the V_{SS} was set to 0 V while the input (A) was swept from 0 to 2 V and the output (Y) was connected to a voltmeter to obtain its voltage transfer characteristics (VTC).

Figure 5 shows the VTC of a single CMOS inverter manufactured using SOI technology at different V_{BG} bias values. From the black colored curve of figure 5, ($V_{BG} = 0 \text{ V}$), it can be established that for low values of the input voltage (V_A), the output voltage (V_Y) is high (2 V). Whereas for high values of V_A , V_Y is low (0 V) which is in accordance with the truth table of an inverter. On the input and output axes, several important voltages and terms are defined as given below:

The voltage output low (V_{OL}) is defined as output voltage for a valid "0". The voltage output high (V_{OH}) is defined as output voltage for a valid "1". The voltage input low (V_{IL}) is defined as smaller input voltage at slope = -1 . The voltage input high (V_{IH}) is defined as larger input voltage at slope = -1 . An important parameter called the noise margin (NM) for the CMOS inverter is defined as the amount of noise that a CMOS circuit can withstand without compromising the operation of the circuit. Noise margin (high) is defined as,

$$N_{MH} = V_{OH} - V_{IH} \text{ (Equation 3)}$$

Similarly, Noise margin (low) is defined as,

$$N_{ML} = V_{IL} - V_{OL} \text{ (Equation 4)}$$

In this case (Figure 5), $V_{OH} = V_{DD} = 2 \text{ V}$, $V_{IH} = 1.25 \text{ V}$, $V_{OL} = 0 \text{ V}$ and $V_{IL} = 0.5 \text{ V}$. Thus, $N_{MH} = 0.75 \text{ V}$ and $N_{ML} = 0.5 \text{ V}$.

The curves on the right side of the black colored curve are for the decreasing negative values of V_{BG} ($-5 \leq V_{BG} \leq -20 \text{ V}$). In this region, the V_{TH} of the PMOS transistor is strongly influenced by the V_{BG} (Figure 4(B)) as it moves towards strong inversion while the NMOS transistor is not influenced as it is in strong accumulation. However, as V_{BG} increases to more negative values ($> -20 \text{ V}$), the PMOS transistor can no longer be turned OFF. As a result, the VTC of the inverter circuit also ceases to reach the V_{IH} value (Figure 5 ($V_{BG} = -15 \text{ V}$ (orange color) and $V_{BG} = -20 \text{ V}$ (pink color))). Similarly, the curves on the left side of the black colored curve are for the positive increasing values of V_{BG} ($5 \leq V_{BG} \leq 20 \text{ V}$). In this region, the V_{TH} of the NMOS transistor is strongly influenced by the V_{BG} (Figure 4(C)) as it moves towards strong inversion while the PMOS transistor is not influenced as it is in strong accumulation. However, as V_{BG} increases to more positive values ($> 10 \text{ V}$), the NMOS transistor can no longer be turned OFF. As a

result, the VTC of the inverter circuit also ceases to reach the V_{OH} value of 2 V (Figure 5 ($V_{BG} = 15$ V (blue color) and $V_{BG} = 20$ V (cyan color))).

The V_{IH} of the inverter linearly increases for negative values of V_{BG} (-5 V $\leq V_{BG} \leq -10$ V). As a result, the N_{MH} (equation 2) linearly decreases by 50 mV per -1 V decrease in V_{BG} . Similarly, the V_{IL} of the inverter linearly decreases for positive values of V_{BG} (5 V $\leq V_{BG} \leq 10$ V). As a result, the N_{ML} (equation 3) linearly decreases by 50 mV per 1 V increase in V_{BG} .

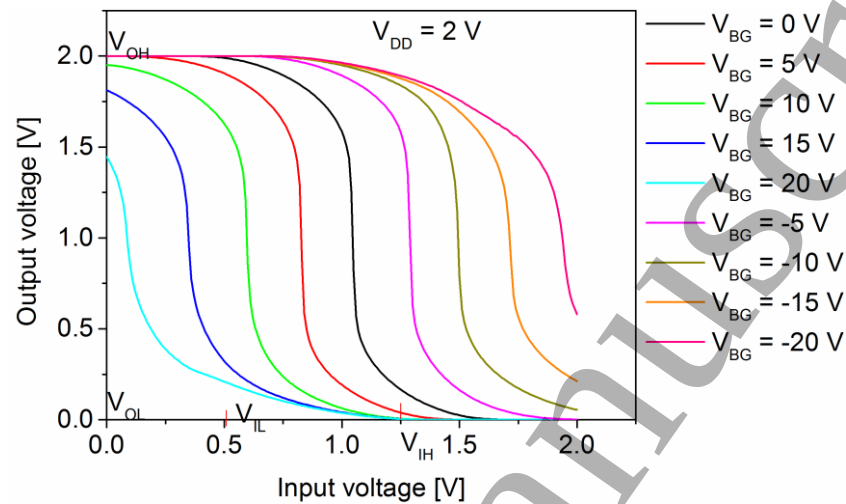


Figure 5. VTC of a single CMOS inverter manufactured using SOI technology at different V_{BG} bias values. The VTC characteristics of the CMOS inverter is preserved for -10 V $\leq V_{BG} \leq 10$ V.

As a conclusion from Figure 5, it can be established that even though the N_{MH} and N_{ML} of the inverter is influenced by the application of the V_{BG} , the VTC characteristics of the CMOS inverter is preserved for -10 V $\leq V_{BG} \leq 10$ V. The application of larger backgate bias voltages such as 15 V $\leq V_{BG} \leq 20$ V and -15 V $\leq V_{BG} \leq -20$ V leads to poor N_{MH} and N_{ML} and deteriorated VTC characteristics of the inverter. Therefore, from CMOS circuit efficiency point of view, it is also important to ensure that the V_{BG} value required to operate the SiNW sensors connected to the output of the pixel device is a small value (5 V $\leq V_{BG} \leq 10$ V for N-type and -5 V $\leq V_{BG} \leq -10$ V for P-type sensors).

3.3 Experimental results before opening access to the SiNW test site

3.31 Backgate mode of operation or I_D - V_{BG} transfer characteristics of N and P-type SiNW pixel sensors

Figure 6 shows the wafer scale backgate mode I_D - V_{BG} transfer characteristics (before opening access to the SiNW test site) of standalone P and N-type SiNW pixel devices ($L = 6$, 2 and 1 μ m and $W = 60$ nm) respectively with frontgate voltage of the control transistor fixed at 0 V.

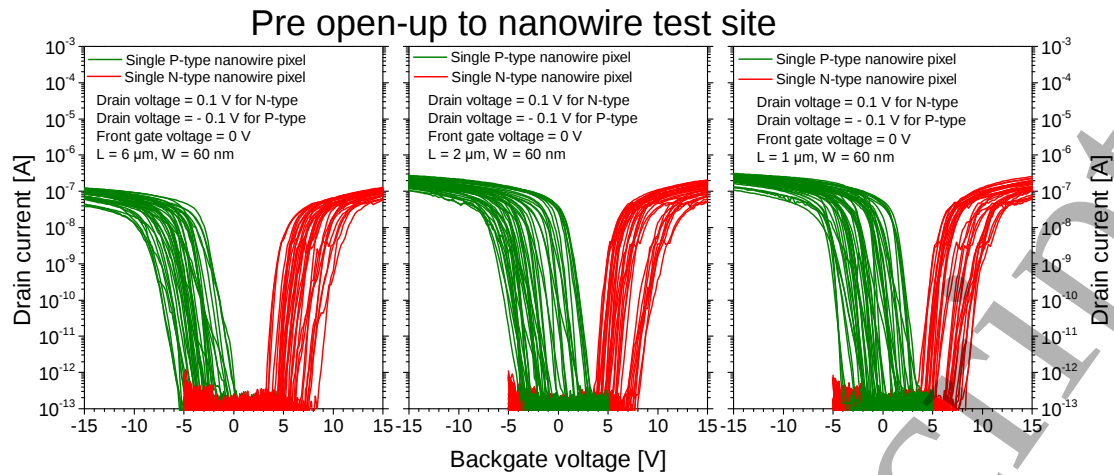


Figure 6. Wafer scale I_D - V_{BG} backgate mode transfer characteristics of standalone P and N-type SiNW pixel devices ($L = 6, 2$ and $1 \mu\text{m}$ and $W = 60 \text{ nm}$) respectively with frontgate voltage of the control transistor fixed at 0 V . These measurements were performed before opening access to the SiNW test site.

In Figure 6, the N-type pixels conduct a current of value $\geq 10 \text{ nA}$ from the source to the drain region when $V_{BG} \geq 10 \text{ V}$ while the current values drop to a value of $\leq 1 \text{ pA}$ when the V_{BG} is decreased to values lesser than 10 V . This confirms that the SiNW pixels exhibit characteristics similar to the N-type MOSFETs. The N-type pixel is turned ON if the control transistor is biased in the inversion region ($V_G = 0 \text{ V}$). Similarly, the P-type pixels conduct a current of value $\geq 10 \text{ nA}$ from the source to the drain region when $V_{BG} \geq -6 \text{ V}$ while the current values drop to a value of $\leq 1 \text{ pA}$ when the V_{BG} is increased to values greater than -5 V . This confirms that the SiNW pixels exhibit characteristics similar to the P-type MOSFETs. The P-type pixel is turned ON if the control transistor is biased in the inversion region ($V_G = 0 \text{ V}$). A SS value of $100\text{-}150 \text{ mV/dec}$ and $I_{ON}/I_{OFF} \geq 10^6$ was noted for both N and P-type pixels. The V_{TH} of the N-type pixel was found to range from 5 to 7 V while the V_{TH} of the P-type pixel was found to range from 2 to -5 V .

3.32 Frontgate mode of operation or I_D - V_G transfer characteristics of N and P-type SiNW pixel sensors

Figure 7 shows the wafer scale I_D - V_G frontgate mode transfer characteristics of single N and P-type SiNW pixel devices of $W = 60 \text{ nm}$ with varying lengths $L = 6, 2$ and $1 \mu\text{m}$ before opening access to the SiNW test site. Since the N and P-type SiNWs are in inversion region of operation for V_{BG} of value $+10 \text{ V}$ and -10 V respectively (Figure 6), the I_D - V_G measurements (frontgate mode) of the SiNW pixels were performed at $V_{BG} = 10 \text{ V}$ for N-type nanowire pixels and $V_{BG} = -10 \text{ V}$ for P-type nanowire pixels respectively (Figure 7). The wafer scale I_D - V_G transfer characteristics of standalone N and P-type control transistor devices of $W = 4 \mu\text{m}$ and $L = 1 \mu\text{m}$ that were connected to the pixel sensors is shown in figure 4(A). From figure 7, it can be established that the N and P-type pixels have similar characteristics to that of N and P-type MOSFET respectively.

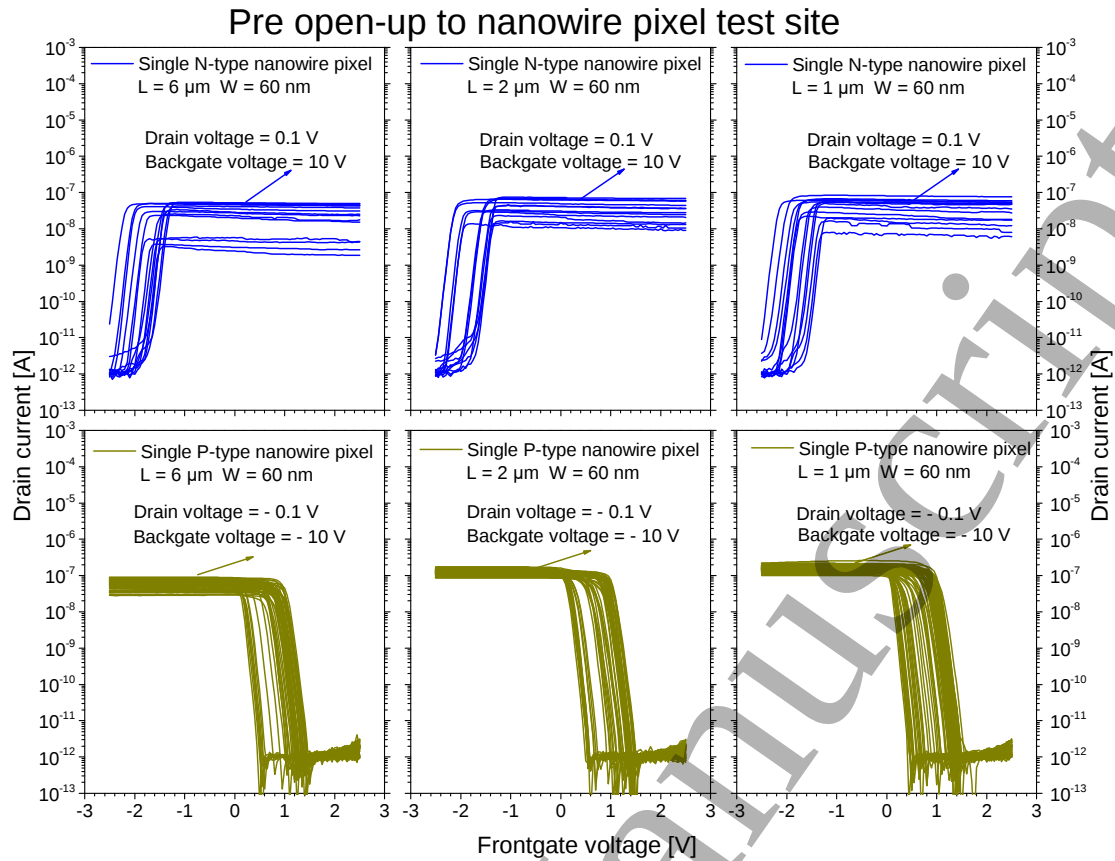


Figure 7: Wafer scale I_D - V_G frontgate mode transfer characteristics of single N and P-type nanowire pixel devices of $W = 60$ nm with varying lengths $L = 6, 2$ and 1 μm before opening access to the SiNW test site. To turn ON the SiNW, the backgate voltage (V_{BG}) is set to 10 V for N-type pixel and -10 V for P-type pixel.

In figure 7, the three different types of N-type pixels ($L = 6, 2$ and 1 μm) conduct a current of value ≥ 1 nA from the source to the drain region when $V_G \geq -2$ V while the current values drop to a value of ≤ 1 pA when the V_G is decreased to values lesser than -2 V. This confirms that the SiNW pixels exhibit characteristics similar to the N-type MOSFETs. The N-type pixel is turned ON if the SiNW sensor is biased in the inversion region ($V_{BG} = 10$ V). Similarly, in figure 7, the three different types of P-type pixels ($L = 6, 2$ and 1 μm) conduct a current of value ≥ 10 nA from the source to the drain region when $V_G \leq 1.5$ V while the current values drop to a value of ≤ 1 pA when the V_G is increased to values greater than 2 V. This confirms that the SiNW pixels exhibit characteristics similar to the P-type MOSFETs. The P-type pixel is turned ON if the SiNW sensor is biased in the inversion region ($V_{BG} = -10$ V). A SS value of 70 - 80 mV/dec and $I_{ON}/I_{OFF} \geq 10^5$ was noted for both N and P-type pixel devices.

From figure 4(A), it can be noted that N-type standalone transistors have an average V_{TH} of ≈ 0 V and variation of ± 0.3 V. However, in figure 7 it can be noted that the V_{TH} of the N-type pixel sensors is ≈ -1.7 V and variation of ± 0.3 V. Most importantly, the V_{TH} of the single N-type pixel sensors is shifted further to the left side from the V_{TH} of the N-type transistors (figure 4(A)). This can be understood from figure 4(C). Since a bias voltage of 10 V was applied to the substrate (V_{BG}) to turn ON the N-type SiNW, the V_{TH} of the N-type transistor shifts further to the left side from its ideal operating condition at $V_{BG} = 0$ V as it moves towards strong

inversion. Similarly, from figure 4(A), it can be noted that P-type standalone transistors have an average V_{TH} of ≈ -1.1 V and variation of ± 0.1 V. However, in figure 7, it can be noted that the V_{TH} of the single P-type pixel sensors is ≈ 0.85 V and variation of ± 0.3 V. Most importantly, the V_{TH} of the P-type pixel sensors is shifted further to the right side from the V_{TH} of the P-type transistors (figure 4(A)). This can be understood from figure 4(B). Since a bias voltage of -10 V was applied to the substrate (V_{BG}) to turn ON the P-type SiNW, the V_{TH} of the P-type transistor shifts further to the right side from its ideal operating condition at $V_{BG} = 0$ V as it moves towards strong inversion. Thus, from this behavior of the N and P-type pixels, it can be concluded that the operating voltage of the monolithically integrated SiNW sensors with CMOS transistors directly depends on the V_{TH} of the standalone SiNW sensors. If the individual SiNW's require larger voltages (> 15 V for N-type SiNW and < -20 V for P-type) to turn ON, then the SiNW pixels cannot be turned OFF. This is on account of the transistors controlling the SiNW sensors operating in strong inversion region. Further, the V_{TH} of the individual SiNW sensors depends on the thickness and quality of the BOX layer in the SOI wafer. Since the BOX layer, is relatively thick (145 nm), the voltage required to turn ON and turn OFF the standalone SiNW sensors is also very high (10 V for N-type and -10 V for P-type SiNW). Also, the fixed charges in the BOX layer will significantly impact the V_{TH} of the standalone SiNW as well as SiNW pixel sensors. A relatively small change of fixed charges of $3 \times 10^{11} \text{ cm}^{-2}$ would induce a V_{TH} shift of 2 V due to the BOX thickness of 145 nm. This issue of large V_{TH} value and corresponding variation between devices can be overcome by employing SOI wafers with a thinner high-quality BOX layer or by replacing the thick BOX layer with a metal backgate.

Furthermore, it is worth noting that the N and P-type pixels in the frontgate mode have low SS (70 – 80 mV/dec) and V_{TH} variation (Figure 7) compared to their operation in the backgate mode (Figure 6). This is on account of the N and P-type pixels in the frontgate mode inheriting the SS and V_{TH} variation from its respective control transistor. Whereas, in the backgate mode, the control transistor is biased at a fixed frontgate voltage ($V_G = 0$ V) and does not influence the SS and V_{TH} of the N and P-type pixels. Therefore, in the backgate mode, the SS and V_{TH} variation of the N and P-type pixel is larger.

According to MOSFET device physics, the drain current of a PMOS device in accumulation (large V_{DS}) can be expressed as a function of width and length of the device as

$$I_{DSsat} \cong \frac{W}{2L} \mu_p C_{ox} (V_G - V_{th})^2 \quad (\text{Equation 5})$$

in the saturation regime (large V_{DS}), and

$$I_{DSlin} \cong \frac{W}{2L} \mu_p C_{ox} (V_G - V_{th}) \cdot V_{DS} \quad (\text{Equation 6})$$

in the linear regime (low V_{DS}). I_{DSsat} is sometimes referred to as I_{ON} . In equations 5 and 6, W is the width of the device, L is the length of the device, μ_p is the hole mobility, C_{ox} is the capacitance of the oxide layer, V_G is the gate voltage, V_{DS} is the

potential difference between source and drain, V_{th} is the threshold voltage of the device. In the absence of any geometrical dependence of mobility, gate surface capacitance and threshold voltage, it is expected from equations 5 and 6 that the drain current at given bias voltages scales directly as a function of the width and inversely as a function of the length.

Figure 8(A) and figure 8(B) shows the wafer scale plot of I_D as a function of length for N and P-type pixels in frontgate and backgate mode respectively. In both cases, I_D decreases linearly as the length of the device increases which is in accordance with equation 5. The error bars in figure 8 are the minimum and maximum values of I_D .

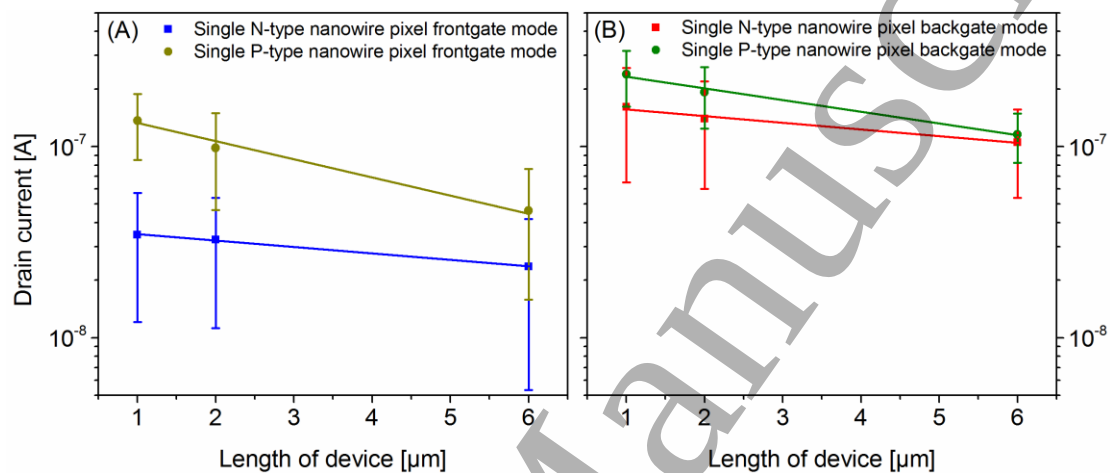


Figure 8. Wafer scale plot of drain current (I_D) as a function of length for N and P-type nanowire pixel devices (A) frontgate mode (B) backgate mode. The error bars in the plot are the minimum and maximum values of the drain current. The current decreases linearly as the length of the device increases.

3.4 Experimental results after opening access to the SiNW test site

The single N and P-type pixels were also electrically characterized after opening access to the sensor test site (see supplementary information). From figure A3 and figure A4, it is established that the SS , I_{ON}/I_{OFF} , V_{TH} variation is well preserved and matches the device characteristics before opening access to the SiNW test site (Figure 6 and Figure 7). This confirms that the electrical and physical integrity of the SiNW pixels is preserved after opening access to the SiNW test site. At this stage, it is worth noting that the N and P-type transistors in the pixel modules that control the SiNW sensors are still passivated with 400 nm SiO_2 and access is only provided to the SiNW test site (Figure A2(B)). This ensures that the surrounding metal lines and circuits are passivated from the liquid or bio environment.

3.5 Influence of backgate voltage on the SiNW pixel sensors in frontgate mode

The V_{TH} of the SiNW pixel in frontgate mode can be tuned to match with the

operating voltage of the control transistors and surrounding CMOS circuits by varying the backgate voltage. Figure 9(A) shows the I_D - V_G frontgate mode transfer characteristics of the single P-type SiNW pixel device of $W = 60$ nm and $L = 6$ μ m at different V_{BG} (-18 V $\leq V_{BG} \leq 0$ V). A systematic V_{TH} shift of ≈ -0.2 V is observed for -1 V change in V_{BG} . The I_D of the pixel also increases by $\approx 10 - 15$ nA for -1 V change in V_{BG} . Likewise, figure 9(B) shows the I_D - V_G frontgate mode transfer characteristics of a single N-type SiNW pixel device of $W = 60$ nm and $L = 6$ μ m at different V_{BG} (6 V $\leq V_{BG} \leq 16$ V). A systematic V_{TH} shift of ≈ 0.2 V is observed for 1 V change in V_{BG} . The I_D of the pixel also increases by $\approx 3 - 4$ nA for 1 V change in V_{BG} .

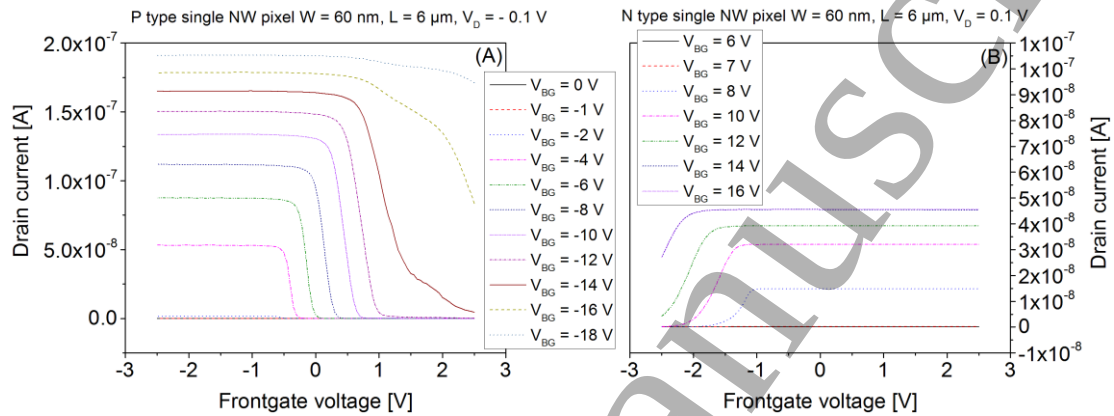


Figure 9. I_D - V_G frontgate mode transfer characteristics of (A) single P-type nanowire pixel (B) single N-type nanowire pixel device of length $L = 6$ μ m and width $W = 60$ nm at different backgate voltages (V_{BG}). In figure 9 (A), a systematic V_{TH} shift of ≈ -0.2 V is observed for -1 V change in V_{BG} . The output drain current (I_D) of the P-type pixel also increases by $10 - 15$ nA for -1 V increase in V_{BG} . In figure 9 (B), a systematic V_{TH} shift of ≈ 0.2 V is observed for 1 V change in V_{BG} . I_D of the N-type pixel also increases by $\approx 5 - 10$ nA for 1 V change in V_{BG} .

Note that in figure 7 and figure 9, the frontgate voltage (V_G) of the N and P-type pixels is swept from -2.5 to 2.5 V. Further increase of the frontgate voltage than the aforementioned range (-2.5 to 2.5 V) will lead to the dielectric breakdown (5 nm SiO_2) in the control transistors. Thus, from this dependence of the N and P-type SiNW pixels (Figure 7 and Figure 9) on V_{BG} , it can be concluded that in the backgate mode it is important to restrict the V_{TH} of the N and P-type SiNW connected to the output of the control transistor to low values (5 V $\leq V_{BG} \leq 10$ V for N-type and -5 V $\leq V_{BG} \leq -10$ V for P-type pixel sensors). The SiNW pixel sensors can be switched ON or OFF if the V_{BG} value required to turn ON the standalone SiNW sensors is within the operating bounds (-2.5 to 2.5 V) of the transistor controlling them. Otherwise, the large V_{BG} value applied to turn ON the standalone SiNW sensors, will push the controlling transistor in the SiNW pixel device towards stronger inversion region of operation. In this regime, the influence of backgate voltage (V_{BG}) is greater than that of the frontgate (V_G). As a result, the SiNW pixel devices cease to switch OFF. The thickness and quality of the BOX layer will also strongly influence the V_{BG} required to bias the standalone SiNW sensors as discussed in previous section 3.32.

3.6 Influence of frontgate voltage on the SiNW pixel sensors in backgate mode

The SiNW sensing principle is based on the detection of changes in the surface charge. However, the surface of the SiNW can also be impacted by interface charges. This leads to unstable devices and erroneous bio detection signals. Therefore, the stability of SiNW pixels in backgate mode operation was also verified by dual sweeping the backgate voltage from 0 V to -15 V for P-type pixels (and 0 to 20 V for N-type pixels) while the front gate voltage was incremented in steps of 0.5 V (-2.5 V to 2.5 V). The goal of the dual sweep measurements was to determine the hysteresis (if any) arising on account of interface traps and establish the stability of the SiNW pixel devices. Figure 10 shows the I_D - V_{BG} backgate mode transfer characteristics of a single P-type and N-type SiNW pixel device of length $L = 6 \mu\text{m}$ and width $W = 60 \text{ nm}$ at different V_G .

It is found that for stable operation of the P-type pixels, the V_G of the P-type control transistor must be in the range from 0 V to -2.5 V (Figure 10(A)). Likewise, from Figure 10(B), it is found that for stable operation of the N-type pixels, the V_G of the N-type control transistor must be in the range from -0.5 V to 2.5 V. Further, in the backgate mode stable region of operation of the N and P-type pixels, negligible hysteresis $\leq 20 \text{ mV}$ was observed after performing dual sweep measurements. This confirmed highly stable SiNW pixel devices. Furthermore, in the stable region of operation of the pixel devices, the changes in V_G was not found to strongly influence the operation of the pixel devices. Thus, it was concluded that the influence of V_G of the control transistors on the SiNW pixel sensors in backgate mode operation is contrary to the results seen in frontgate mode operation (Figure 9). In the frontgate mode operation, incremental changes in backgate voltage was strongly impacting the I_D , SS and V_{TH} of the SiNW pixels while similar observations were not recorded in the backgate mode operation.

It is worthwhile to note that in figure 10 (B), for the curves at $-2.5 \text{ V} \leq V_G \leq -1 \text{ V}$, the I_D - V_{BG} characteristics saturate initially. But, at higher backgate voltages $V_{BG} \geq 15 \text{ V}$, the drain current starts to increase. We speculate this behavior to arise on account of the partial conducting nature of the N-type control transistor in the regime $-2.5 \text{ V} \leq V_G \leq -1 \text{ V}$ (Figure 4C and Figure 7). Whereas, such a behavior is absent for the curves at $-0.5 \text{ V} \leq V_G \leq 2.5 \text{ V}$ because the transistor is completely turned ON (Figure 4C and Figure 7).

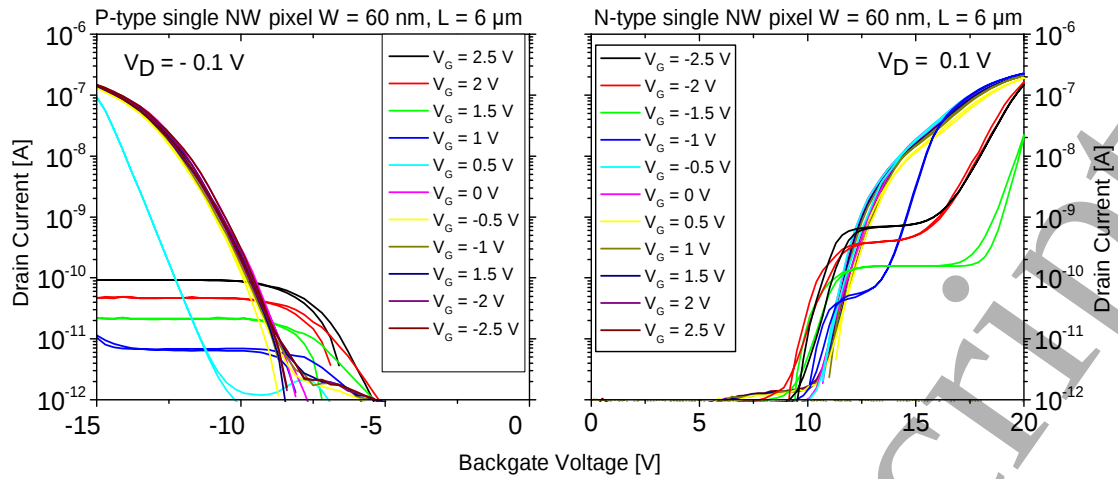


Figure 10. I_D - V_{BG} backgate mode transfer characteristics of single (A) P-type (B) N-type SiNW pixel device of length $L = 6 \mu\text{m}$ and width $W = 60 \text{ nm}$ at different V_G . For stable operation of the P and N-type pixels the V_G of the P and N-type control transistors have to be in the range $0 \text{ V} \leq V_G \leq -2.5 \text{ V}$ and $-0.5 \text{ V} \leq V_G \leq 2.5 \text{ V}$ respectively.

Conclusion

In this article, the monolithic integration of SiNW sensor with CMOS has been realized using a novel pixel-based LOC architecture. A single pixel sensor comprised of a control MOSFET, an on-chip fluid-gate and a SiNW sensor connected at its output. The top-down STL method of fabrication was exploited to manufacture the SiNW pixels. Wafer scale integration was exposed on 100 mm SOI substrate using the CMOS industry grade materials and tools.

Further, we demonstrated the first electrical results of the pixel design for both N and P-type SiNW pixels in two different modes – a) the backgate mode b) the frontgate mode. From the I_D - V_{BG} characteristics in the backgate mode, it is found that the N or P-type pixels exhibit similar characteristics to that of N and P-type MOSFETs respectively with a SS of 100-150 mV/dec and $I_{ON}/I_{OFF} \geq 10^6$. Likewise, the I_D - V_G frontgate mode transfer characteristics of N and P-type SiNW pixel devices was noted to be similar to the I_D - V_G transfer characteristics of N and P-type MOSFETs respectively with a SS of 70-80 mV/dec and $I_{ON}/I_{OFF} \geq 10^6$. However, in comparison with the backgate mode, the SS and V_{TH} variation in the frontgate operation was relatively low as the N and P-type pixels in the frontgate mode inherit the SS and V_{TH} variation from its respective control transistor.

We also show the influence of different V_{BG} bias on the I_D - V_G frontgate transfer characteristics of a single N and P-type SiNW pixel devices. The tuning of the V_{TH} of the SiNW pixel by using the backgate bias will be useful to match with the operating voltage of the control CMOS circuits. Lastly, we demonstrate the influence of different V_G bias on the I_D - V_{BG} backgate transfer characteristics of a single N and P-type SiNW pixel devices. It is found that for stable operation of the P-type pixels, the V_G of the P-type control transistor must be in the range from 0 V to -2.5 V. Similarly, it is found that for stable operation of the N-type pixels, the V_G of the N-type control transistor must be in the range from -0.5 V to 2.5 V.

Indeed, the novel SiNW pixel-based design and promising transfer characteristics of the pixels will pave the way for LOC technology that addresses the key areas of selective and multiplexed detection of biomarkers.

Author contribution statement:

Conceptualization, G.J.; Formal analysis, G.J.; Funding acquisition, M.Ö.; Investigation, G.J.; Methodology, G.J.; Project administration, M.Ö.; Resources, M.Ö.; Supervision, M.Ö.; Visualization, G.J.; Writing original draft, G.J.; and Writing review and editing, M.Ö.

Conflict of interest

The authors declare no competing financial interests.

Acknowledgements

This work has been supported by the Nanonets2Sense project fund by the European Horizon 2020 Program under grant agreement 688329. MyFab, the Swedish national research infrastructure for micro and nano fabrication, is acknowledged for their contribution.

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