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High-throughput impedance spectroscopy biosensor array chip

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Impedance spectroscopy is a powerful tool for characterizing materials that exhibit a frequency dependent behaviour to an applied electric field. This paper introduces a fully integrated multi-channel impedance extraction circuit that can both generate AC stimulus signals over a broad frequency range and also measure and digitize the real and imaginary components of the impedance response. The circuit was fabricated in a 0.5 μm complementary metal-oxide semiconductor. Tailored for cellular membrane interface characterization, the signal generator produces sinusoidal waves from 10 mHz to 10 kHz. To suit a variety of applications, the impedance extraction circuit provides a programmable current measurement range from 100 pA to 100 nA with a measured resolution of approximately 100 fA. Occupying only 0.045 mm^2 per measurement channel, the circuit is compact enough to include nearly 200 channels in a 3×3 mm^2 die area.

1. Introduction

Impedance biosensors measure the biointerfacial impedance change caused by biorecognition events. Impedance techniques are widely used in lipid bilayer monitoring [1–4], DNA testing [5], small molecules of biological relevance [6,7] and cell presence or cell concentration detection etc. [8,9]. An impedimetric biosensor is accomplished by imposing a small sinusoidal voltage over a range of frequencies and measuring the resulting current, which is referred to as the impedance spectroscopy (IS) technique. The phase and amplitude of the sinusoidal wave applied to the electrode–electrolyte interface would shift when biorecognition events occur.

Due in part to the progress being made in complementary metal-oxide semiconductor (CMOS) compatible

fabrication of microelectrodes [10], there is a trend to build high-throughput biosensor arrays that deposit multiple miniaturized biosensors on the surface of silicon chips and interrogate these biosensor elements with on-chip electronics [5,11]. High-throughput biosensor array methods allow rapid, direct and quantitative detection of a wide range of bimolecules [12,13]. To support chip-scale high-throughput impedance array applications, a very hardware efficient and low power solution is needed that combines accurate, low noise impedance measurement circuits with electronics capable of extracting phase and amplitude components to circumvent the heavy signal processing load involved in parallel impedance extraction of a biosensor array [11].

A number of impedance measurement systems have been built for miniaturized biomedical and biochemical systems [1,14–18]. A conversion receiver without an on-chip ADC [17] extracts impedance with 104 mW power consumption. A single-channel impedance extractor based on a lock-in amplifier that extracts the sensor impedance was developed [18]. A 16-channel IS DNA analyser with dual-slope multiplying ADC was presented [14]. However, these reported IS chips are not suitable for a high-throughput array because of their large area or high-power consumption.

To overcome these limitations, our group recently reported a low power impedance to digital converter circuit that has the capability to integrate 100 readout channels in a $3 \times 3\,\mathrm{mm}^2$ die area [1]. Building on this past work, this paper presents a new impedance spectrum array (ISA) chip that maintains the high performance of its predecessor while adding a stimulus signal generator and significantly decreasing the readout circuit area to enhance measurement throughput in biosensor arrays. The ISA chip includes a digitally programmable sinusoidal frequency synthesizer (SFS) and multiple channels of a compact impedance readout circuit (IRC). The IRC cell includes analogue domain impedance extraction and local digitization while remaining compact enough to be instantiated for each sensor element, enabling massively parallel IS interrogation. The ISA chip was combined with an electrode array fabricated on the CMOS chip to form a monolithic measurement system.

In this paper, the IS method is introduced in §2. The CMOS implementation of the ISA circuitry is presented in §3. Section 4 describes post-CMOS electrode microfabrication and packaging for liquid environments. Test results are presented in §5 followed by a conclusion.

2. Impedance spectroscopy methods

For impedance biosensors, biorecognition events alter the phase and amplitude of the stimulus signal in a manner that is algebraically related to real and imaginary components of the sensor's instantaneous impedance. The phase and amplitude shift caused by biorecognition can be extracted in the digital domain using a fast Fourier transform (FFT) algorithm [19] that uses a broadband stimulus, for example a pulse, and computes the result at all frequency points simultaneously, producing an impedance spectrum. The composite signal source and the computationally intensive Fourier transform require FFT-based IS instrumentation to use a digital signal processor (DSP) with extensive computational resources [20]. Alternatively, in the analogue domain, sensor phase and amplitude can be extracted using the frequency response analyser (FRA) method. FRA processes the response of one frequency point at a time as it sweeps over the frequency range of interests. Compared to FFT, the FRA method can be realized with simple and compact analogue circuits, making it more suitable for biosensor arrays [20]. As a result, most of the reported CMOS impedance extraction circuits have used FRA methods [14,17,18,21–24].

In the FRA-based impedance measurement method, a sinusoidal stimulus signal with known frequency is applied to the sensor interface. Thus, two main functional blocks are needed in FRA IS instrumentation: a SFS and an IRC. The SFS serves to generate a sinusoidal stimulus with programmable frequency and amplitude, and the IRC extracts the phase/amplitude or real/imaginary shift.

To achieve phase/amplitude extraction, all reported FRA readout circuits have used the lock-in technique. Lock-in is achieved by multiplying the biosensor's AC response signal with a

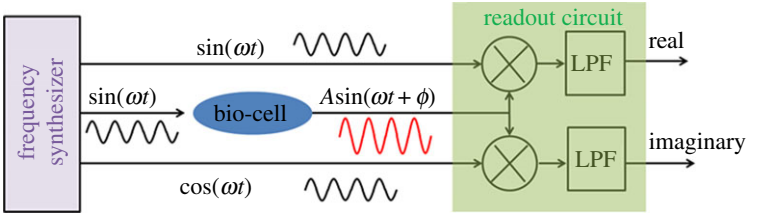

Figure 1. Illustration of the lock-in-based FRA impedance component extraction method. (Online version in colour.)

reference signal matched to the frequency of the stimulus. This multiplication results in a DC output that is proportional to the real/imaginary portions of the AC signal under investigation. Figure 1 illustrates how the lock-in technique extracts phase/amplitude or real/imaginary response components in the lock-in-based FRA algorithm. A frequency synthesizer generates the sinusoidal voltage $\sin(\omega t)$ as stimulus signal. The bio-cell response signal is $A\sin(\omega t + \theta)$ with phase shift θ and amplitude shift A. After multiplying separately with reference signals $\sin(\omega t)$ and $\cos(\omega t)$, the DC component of the products are proportional to the real and imaginary parts, respectively, of the bio-cell response signal. This function can be expressed as

$$A\sin(\omega t + \theta)\sin(\omega t) = \frac{A}{2}[\cos\theta - \cos(2\omega t + \theta)] = \frac{A}{2}\cos(\theta) - \frac{A}{2}\cos(2\omega t + \theta) \overset{\text{LPF}}{\Rightarrow} \frac{1}{2}A\cos(\theta) = \frac{1}{2}\text{Re}_{\text{bio}} \tag{2.1}$$

and

$$A\sin(\omega t + \theta)\cos(\omega t) = \frac{A}{2}[\sin\theta + \sin(2\omega t + \theta)] = \frac{A}{2}\sin(\theta) + \frac{A}{2}\sin(2\omega t + \theta) \overset{\text{LPF}}{\Rightarrow} \frac{1}{2}A\sin(\theta) = \frac{1}{2}\text{Im}_{\text{bio}}, \tag{2.2}$$

where Re_{bio} and the Im_{bio} are the real and imaginary portions of the bio-cell impedance, respectively. ω is the stimulus frequency, and $A\cos(2\omega t + \theta)$ and $A\sin(2\omega t + \theta)$ are higher order frequency components that can be removed by a low pass filter (LPF) [1,24]. Based on (2.1) and (2.2), the amplitude shift A and phase shift θ can be calculated by

$$A = \sqrt{\text{Re}_{\text{bio}}^2 + \text{Im}_{\text{bio}}^2} \tag{2.3}$$

and

$$\varnothing = \tan^{-1}\frac{\text{Im}_{\text{bio}}}{\text{Re}_{\text{bio}}}. \tag{2.4}$$

The reference signals $\sin(\omega t)$ and $\cos(\omega t)$ can be replaced by rectangular waveform having the same phase as $\sin(\omega t)$ and $\cos(\omega t)$ without loss of performance because the higher odd harmonics caused by the rectangular waveform substitution would be eliminated by the included LPF. As a result, no $\cos(\omega t)$ generator is need within the frequency synthesizer, which simplifies the complexity of this circuit. The ISA chip described in this paper uses this lock-in technique with rectangular $\sin(\omega t)$ and $\cos(\omega t)$ reference signals.

3. CMOS implementation

Figure 2 illustrates the biosensor array microsystem that serves as the conceptual model for the work in this paper. The ISA chip acts as the substrate for the microsystem. An array of biosensor electrodes are fabricated post-CMOS on the surface of the chip. The SFS circuit generates stimulus signals for the bio-cell array, and the IRC circuit measures the bio-cells' response signals. The ISA chip communicates with a PC to send control commands and analyse data from the ISA chip. To support measurement in a liquid environment, the ISA chip is packaged using a parylene coating process following post-CMOS deposition of an electrode array on the surface of the chip. The circuitry is described in this section, and the electrode and packaging processes are described in §4.

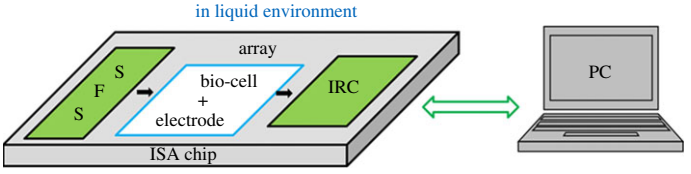

Figure 2. Conceptual illustration of the IS circuit with SFS and IRC circuitry and on-chip electrode and biointerface array. The chip communicates with a PC to upload configuration data and download digitized measurement results. (Online version in colour.)

(a) Frequency synthesizer

Many circuits for sinusoid frequencies have been reported, including a DSP-based solution [25], quadrate oscillators [26,27] and triangle-to-sine generators [28]. The drawback of the DSP-based solution is the large memory requirement for very low frequencies. The limitations of the quadrate oscillators and triangle-to-sine generators are their poor linearity and difficulty in precisely controlling frequency. Our group reported an alternative method that is controlled purely by digital signals and produces excellent frequency accuracy and linearity [29]. It provides seven orders of frequency-tuning range (1 mHz–10 kHz) appropriate for impedance characterization of many biosensor interfaces. This SFS topology employs a hybrid architecture, integrating two different structures, one for low frequencies and one for high frequencies, to accurately cover a wide range of frequencies. For high frequency (above 100 Hz), an unevenly tipped resistor chain with tunable updating clock was employed. At lower frequency (below 100 Hz), a subsampling method was used.

The SFS reported in this paper is based on our reported hybrid structure. However, by using rectangular waveform reference $\sin(\omega t)$ and $\cos(\omega t)$ signals, as described above, the ISA chip eliminates the need for a sinusoidal cosine frequency generator. This permits significant reduction of circuit area, increasing potential density of sensor elements on the chip, without loss of performance. The block diagram of the SFS is shown in figure 3. In the R-chain-based high-frequency sinusoid generator, the resistive DAC (R-DAC) is a 1000 identical unit-value resistor chain with sinusoidally spaced taps. These taps are selected by the output of the token ring in the proper sequence to generate the next sine wave sample. The token ring also determines the state of the digital $\sin(\omega t)$ and $\cos(\omega t)$ (square waveform in phase with $\sin(\omega t)$ and $\cos(\omega t)$). A second-order Butterworth filter was implemented using a g_m-C biquadratic filter to remove high-frequency quantization replicas from the R-DAC output. Its cut-off frequency is adjustable (2 kHz–200 kHz) by programming both the g_m and capacitor values. The R-DAC output is also provided as an input to the subsampling signal generator, which samples this signal at a frequency that is very close to the signal frequency, i.e. the frequency difference is very small. The output of the sampling circuit contains a low-frequency replica that represents the frequency difference between the input signal and the sampling clock. A detailed analysis was presented in [29].

(b) Impedance readout circuit

The IRC presented here is based on the lock-in FRA method described above where the main functional blocks are a multiplier and an LPF. The performance of the LPF is circuital for accurate impedance extraction because the *real* and *imaginary* components are represented by only the DC output. All of the high-frequency harmonic noise after the multiplier has to be removed by the LPF. Thus, an LPF with a low cut-off frequency and a high rate of frequency roll-off is required. To relax the challenge in achieving such difficult requirements, a hybrid method we previously reported [1] was adopted. This method combines the lock-in and oversampling techniques to achieve a high sensitivity IRC. The oversampling technique moves the low-frequency noise to

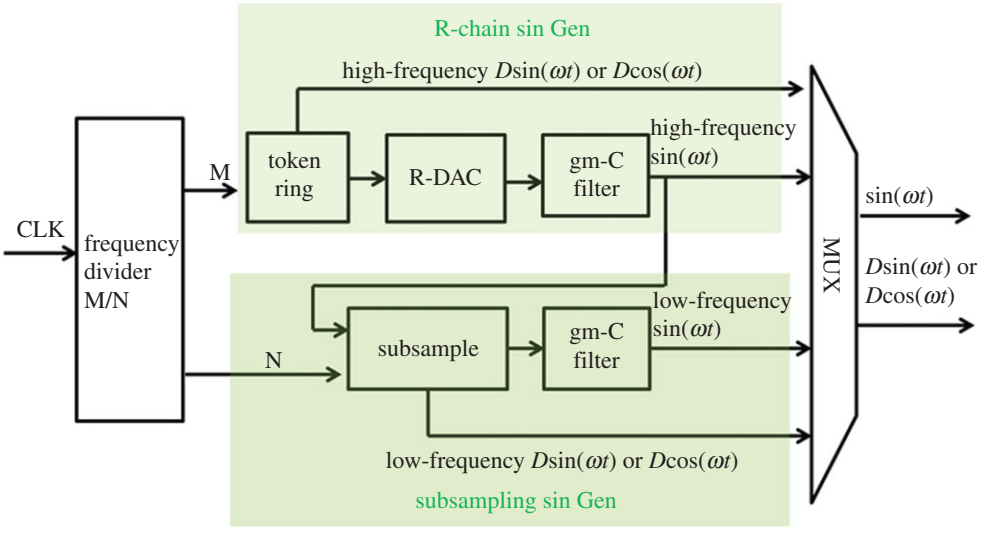

Figure 3. Block diagram of the signal generator that produces stimulus signal sin(ωt) and the reference square wave $D\sin(\omega t)$ and $D\cos(\omega t)$. (Online version in colour.)

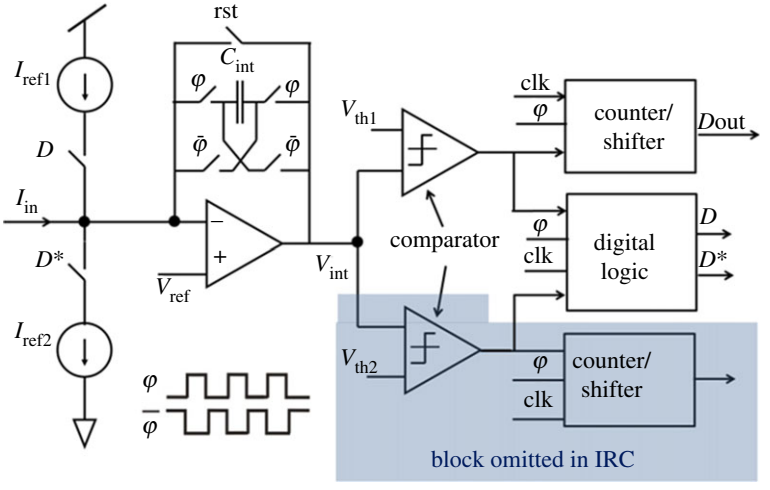

Figure 4. Simplified structure of the impedance readout circuitry presented in [1] and the new IRC that eliminates the shaded portion. φ and not-φ are non-overlapping reference square waves. (Online version in colour.)

high frequency where it can be removed easily by an LPF with less stringent design requirements. The impedance readout circuitry in [1] includes an analogue multiplier, an integrator, two comparators and two bidirectional counters. The integrator achieves the LPF function. The two comparators and two bidirectional counters were used for calibration of the mismatch between two current references. In the new IRC reported here, the current reference mismatch is reduced by increasing the WL size of transistors within the current references. Thus, the DC offset caused by reference mismatch can be calibrated by a digital calibration method and then removed from the digital output [30,31]. As a result, only one comparator and one bidirectional counter are needed in the IRC, as shown in figure 4 along with the additional block from the prior design that has been eliminated to improve hardware efficiency and power consumption.

In the IRC, if the square wave reference $\varphi(t)$ is in phase with $\sin(\omega t)$, then $\varphi(t)$ can be described by

$$\varphi(t) = \mathrm{sgn}(\sin(\omega t)) = \begin{cases} 1, nT \le t < \left(nT + \dfrac{T}{2}\right) \\ -1, \left(nT + \dfrac{T}{2}\right) \le t < (n+1)T, \end{cases} \tag{3.1}$$

where T is the period of the stimulus signal and n is any integer. If the biosensor response current I_{in} is multiplied by (3.1) and integrated over N continuous stimulus cycles, then the integrator's output is given as

$$\begin{aligned} \int_0^{\mathrm{NT}} I_{\mathrm{in}} \cdot \varphi(t)\mathrm{d}t &= \sum_{i=0}^{N-1} \left(\int_{iT}^{(i+1/2)T} I_{\mathrm{in}}\mathrm{d}t - \int_{(i+1/2)T}^{(i+1)T} I_{\mathrm{in}}\mathrm{d}t \right) \\ &= \frac{2T}{\pi} \cdot N \cdot A\cos(\theta) = \frac{2T}{\pi} \cdot N \cdot \mathrm{Re}_{\mathrm{bio}}, \end{aligned} \tag{3.2}$$

where $I_{\mathrm{in}} = A\sin(\omega t + \theta)$. Thus, the *real* component, $\mathrm{Re}_{\mathrm{bio}}$ of the biosensor response signal can be extracted with a multiplier, an integrator and a reference square-wave $\varphi(t)$ that is in phase with $\sin(\omega t)$.

Based on (3.2), if the $\int I_{\mathrm{in}}\mathrm{d}t$ in different integration cycles can be calculated, then the *real* component can be determined. To simplify analysis, assume that $\varphi(t)$ is in phase with $\sin(\omega t)$ and that both comparator results, D and D^*, are low at all of φ's transition edges. If not, the multiplexing switches controlled by φ will force D and D^* to exchange their polarity of charge injection through reference current I_{ref1} or I_{ref2}. From time 0 to $T/2$, φ is high and the counter is counting up. Just before φ's edge at time $T/2$, according to the charge conservation theory, at the input node, we have

$$\int_0^{T/2} I_{\mathrm{in}} \cdot \mathrm{d}t = \mathrm{CV}_{\mathrm{res1}} + I_{\mathrm{ref1}} T_0 \sum_{i=1}^{N/2} D_{\mathrm{i}} - I_{\mathrm{ref2}} T_0 \sum_{i=1}^{N/2} D_{\mathrm{i}}^*, \tag{3.3}$$

where V_{res1} is the residue value at the integrator output, T_0 is the updating clock period and N is the number of clock cycles from time 0 to $T/2$. From time $T/2$ to T, φ is low, the integrator capacitor is reversed and the counter is set to down counting mode. This mode produces

$$\int_{T/2}^{T} I_{\mathrm{in}} \cdot \mathrm{d}t = \mathrm{C}(V_{\mathrm{res1}} + V_{\mathrm{res2}}) + I_{\mathrm{ref1}} T_0 \sum_{N/2+1}^{N} D_{\mathrm{i}} - I_{\mathrm{ref2}} T_0 \sum_{N/2+1}^{N} D_{\mathrm{i}}^*, \tag{3.4}$$

where V_{res2} is the integrator's output voltage at time T. Simplifying the equation with $D^* = 1 - D$ and combining (3.3) and (3.4), the full cycle produces

$$\int_{T/2}^{T} I_{\mathrm{in}} \cdot \mathrm{d}t = -\mathrm{CV}_{\mathrm{res2}} + T_0 \cdot (I_{\mathrm{ref1}} + I_{\mathrm{ref2}}) \left(\sum_{N/2+1}^{N/2} D_{\mathrm{i}} - \sum_{1}^{N/2} D_{\mathrm{i}} \right). \tag{3.5}$$

Thus, the *real* result is represented by the contents of the counter (the summations in (3.5)), provided the circuit parameters are chosen such that $|\mathrm{CVres2}| < 1/2 \min(I_{\mathrm{ref1}} T_0, I_{\mathrm{ref2}} T_0)$ where the residue on the integrator can be treated as noise. If the IRC is operated for N consecutive stimulus cycles after initial reset, the residue term in (3.5) remains in the same range while the digital part is magnified by N. Therefore, the error due to ignoring the residual will decrease with repeated cycles. The *real* component after N cycles can be expressed as

$$\begin{aligned} \mathrm{Re}_{\mathrm{bio}} &= \frac{\pi}{2TN} \cdot \int_0^{NT} I_{\mathrm{in}}(t) \cdot \varphi(t)\mathrm{d}t \\ &= \frac{\pi T_0}{2T} \cdot (I_{\mathrm{ref1}} + I_{\mathrm{ref2}}) \cdot \left(\sum_{N/2+1}^{N} D_{\mathrm{i}} - \sum_{1}^{N/2} D_{\mathrm{i}} \right). \end{aligned} \tag{3.6}$$

Following a similar analysis, it can be shown that the counter will contain the imaginary portion of admittance when $\varphi(t)$ is in phase with $\cos(\omega t)$. The imaginary portion can be presented by

$$\begin{aligned} \mathrm{Im}_{\mathrm{bio}} &= \frac{\pi}{2TN} \cdot \int_0^{NT} I_{\mathrm{in}}(t) \cdot \varphi(t) \mathrm{d}t \\ &= \frac{\pi T_0}{2T} \cdot (I_{\mathrm{ref1}} + I_{\mathrm{ref2}}) \cdot \left(\sum_{N/4}^{3N/4} D_{\mathrm{i}} - \sum_{1}^{N/4} D_{\mathrm{i}} - \sum_{3N/4+1}^{N} D_{\mathrm{i}} \right). \end{aligned} \tag{3.7}$$

Thus, by setting φ to be in or out of phase with the stimulus sinusoid, the IRC circuit can extract both portions of the full impedance using a structure that inherently digitizes the result while sharing resources to minimize size and power. The bidirectional counter also serves as a shift register to permit serial data upload of all channels.

4. On-chip array

To transform the ISA chip into a single-chip impedance measurement biosensor array, electrodes must be fabricated on the CMOS chip surface and the device must be packaged for use within a liquid environment. In prior work [32], we introduced an on-chip electrode fabrication method and packaging scheme for a CMOS electrochemical amperometry circuit. Because the post-CMOS electrode fabrication and packaging requirements of the prior amperometry chip are essentially identical to those of the ISA chip reported here, the same approaches were adopted to implement the impedance measurement biosensor chip. The overall integration procedure is described below in two parts. First, the die-level electrode fabrication is introduced. Second, the packaging method that enables testing in liquid environment is described.

(a) Die-level fabrication

Gold is an outstanding metal to form an on-chip microelectrode array because it can readily be deposited and patterned, is inert and biocompatible in a biosensing liquid environment and permits immobilization of biointerfaces using well-established adhesion chemistry. An electroless nickel immersion gold process could be used to fabricate on-chip electrode, which replaces the aluminium layer from a standard CMOS process [24]. However, it is difficult to control the thickness of gold with this method owing to its deposition mechanism, and the process is prone to poor reproducibility because of variable aluminium alloy composition across a chip and between different chips. Our experimental efforts with this deposition process have resulted in a non-uniform gold layer with high surface roughness. Alternatively, using conventional physical vapour deposition (PVD) and photolithography, the on-chip microelectrode array could be fabricated with precise control of electrode thickness and area. The roughness of the gold is subject to the surface conditions of the CMOS chip, which is typically passivated by a smooth silicon dioxide layer.

The die-level post-CMOS fabrication process begins with formation of the electrode array on the CMOS chip. The electrodes are formed by thermal evaporation of titanium/gold (50 Å/1000 Å) and patterning by wet etching. This metallization step also creates routing between electrodes and surface contacts to CMOS electronics, and it covers all surface CMOS metal, including bondpads, to eliminate chemical reactions between the CMOS aluminium alloy and the alkali photoresist developer, which has been observed to contaminate the surface electrodes. Polyimide is then spin coated on the CMOS chip surface and patterned to insulate surface routings and define the electrode area while leaving bonding pads open for subsequent wire bonding. Polyimide provides good coverage of two-dimensional surfaces and is easy to pattern. The die-level process steps are shown in figure 5. After this process, the electrode array has been formed and the chip surface has been covered everywhere except the desired electrode areas and the wire bond pads.

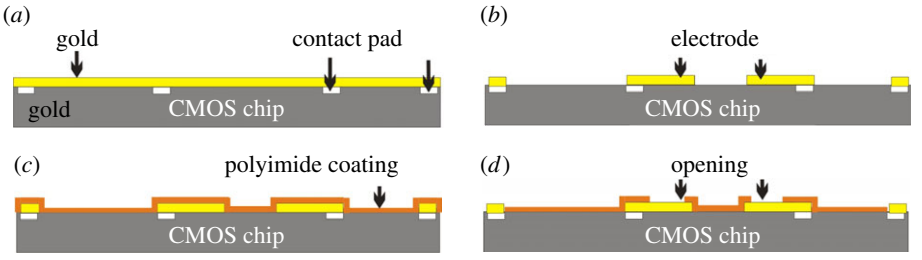

Figure 5. Process flow for post-CMOS electrode fabrication: (*a*,*b*) Ti/Au is deposited and patterned and (*c*,*d*) polyimide is spin coated and patterned. (Online version in colour.)

(b) Package-level fabrication

To allow the chip to be tested in liquid while keeping cost and complexity low, a solution was developed using a chip-in-package approach, where the chip is mounted and wire bonded to a standard ceramic package and the package body is used as a liquid reservoir. Figure 6 describes the package-level post-CMOS process for the chip-in-package approach. Following the die-level processing described above, the CMOS chip is wire bonded to a ceramic package. The packaged chip is then coated with a 5 µm layer of parylene using PVD (PDS 2035CR, Specialty Coating Systems). This process covers all surfaces within the package, including bond wires, package contact pads and the electrode array chip. Next, a hole punch is used to create a cylinder of PDMS, sized to match the area of the chip's surface, from which parylene would be removed, approximately 1.5 mm diameter in this case. A silicon chip of slightly smaller diameter is also cut from a wafer using a dicing saw. The cylinder is then attached, on one side, to the silicon chip using oxygen plasma-assisted bonding and, the other side, to a glass slide. The silicon chip is included to eliminate direct contact of PDMS with parylene, which is observed to leave unwanted particle contaminants that are difficult to remove. The glass slide is then clamped to the parylene-coated chip-in-package with the silicon chip pressed down over the electrode area. Crystal adhesive is then inserted into the cavity beneath the slides and melted at 120°C to fill the cavity except where the PDMS/silicon cylinder is held (figure 6*b*). The slide/PDMS/silicon assembly is then removed leaving parylene everywhere except the interior of chip's surface where previously deposited polyimide remains to insulate surface routing and leave only the electrodes exposed. Parylene is then etched using reactive-ion etching (RIE), with 300 W RF power and 500 sccm oxygen flow rate, to expose the desired electrode surfaces (figure 6*c*). Once the crystal adhesive is removed using acetone, the final package provides exposed electrodes with all other surfaces coated with parylene (figure 6*d*). A PDMS reservoir is then bonded on top of the package to hold enough solution to take measurements (figure 6*e*).

5. Test result

The ISA chip was fabricated in a standard 0.5 µm CMOS process, and photographs of the parylene-packaged chip with 10 × 10 on-chip electrode array are shown in figure 7. The diameter of each on-chip electrode is 100 µm. One SFS and 26 IRC channels have been integrated on the $3 \times 3\,\text{mm}^2$ chip. The area of each IRC channel is $0.045\,\text{mm}^2$, which is 25% less than the area of the circuit reported in [1]. The performance of the SFS matched the original version reported in [29], with a spurious-free dynamic range of the generated sinusoid at more than 50 dB and a total harmonic distortion of less than 0.6% in the 1 mHz–10 KHz frequency range.

To characterize the circuit's response to variable impedance, an IRC channel output was recorded while independently changing the phase and amplitude of the stimulus input. Ideally, the relationship between the input signal's amplitude and the digitized *real* component output is linear for a constant phase and frequency. To verify the amplitude transfer function, a 10 Hz,

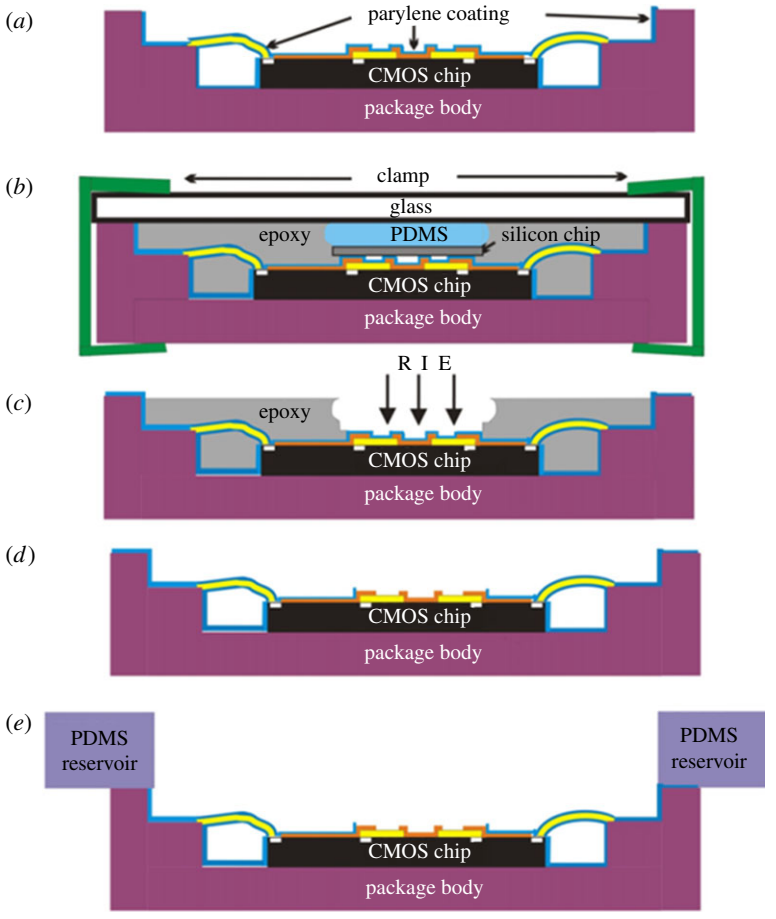

Figure 6. Process flow of chip-in-package sealing for liquid environment. (*a*) Chip is wire-bonded to package and coated by 5 μm parylene. (*b*) A PDMS cylinder and silicon chip are attached to a glass slide and clamped to the package to cover the centre of the CMOS chip before crystal adhesive is melted to fill the cavity. (*c*) The glass slide is detached and parylene is etched away by oxygen RIE. (*d*) Crystal adhesive is removed to form the final package with all non-electrode surfaces insulated. (*e*) PDMS forms a reservoir on top of a CMOS chip. (Online version in colour.)

zero initial phase sinusoid signal was supplied with amplitude swept from 0 to 10 nA. The IRC digital output data were recorded by data acquisition card (DAQ6259). The calculated differential nonlinear (DNL) and integral nonlinear (INL) characteristics of the digitized *real* portion output are plotted in the figure 8, which shows that the *real* portion dynamic range is more than 50.2 dB for the 10 nA input range.

The relationship between the input signal's phase and the digitized *imaginary* component output is theoretically a sine wave for a constant amplitude and frequency. To measure the phase transfer function, a cosine input with constant 100 Hz frequency, constant 3 nA amplitude and variable phase was supplied. The normalized digitized *imaginary* portion output is plotted in figure 9. The output fits the expected sine wave with an RMS error of only 0.02.

The IRC block was designed to operate in five digitally selectable input current ranges to extend operation over a wide input range. The maximum current for each range is 100 nA, 10 nA, 1 nA, 100 pA and 10 pA. Operation was verified for all ranges. The maximum current resolution (based on DNL/INL measurements at each range) scales with the current range, having a value of approximately 300 pA in the largest 100 nA range. The dynamic range decreases in the low current ranges with the maximum current resolution of approximately 100 fA in the lowest 10 pA range. A performance summary of the ISA chip is presented in table 1.

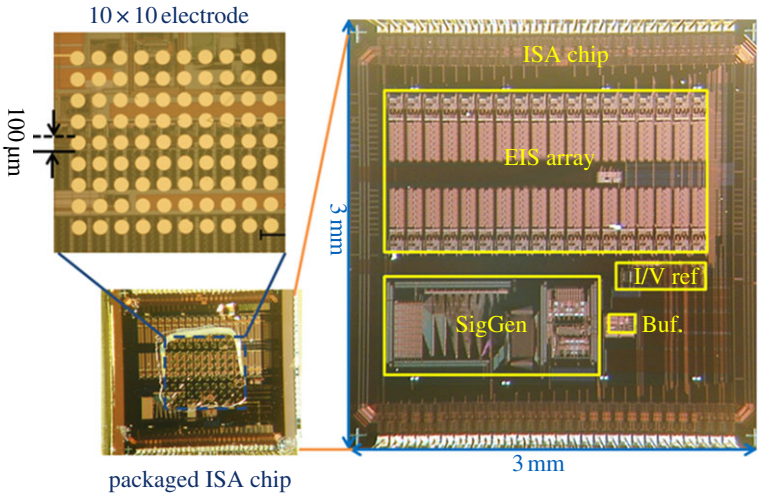

Figure 7. Photographs of the ISA chip in packaging for liquid environment. ISA die (without on-chip electrode for clearer view) and close up views of the on-chip gold electrode are included. (Online version in colour.)

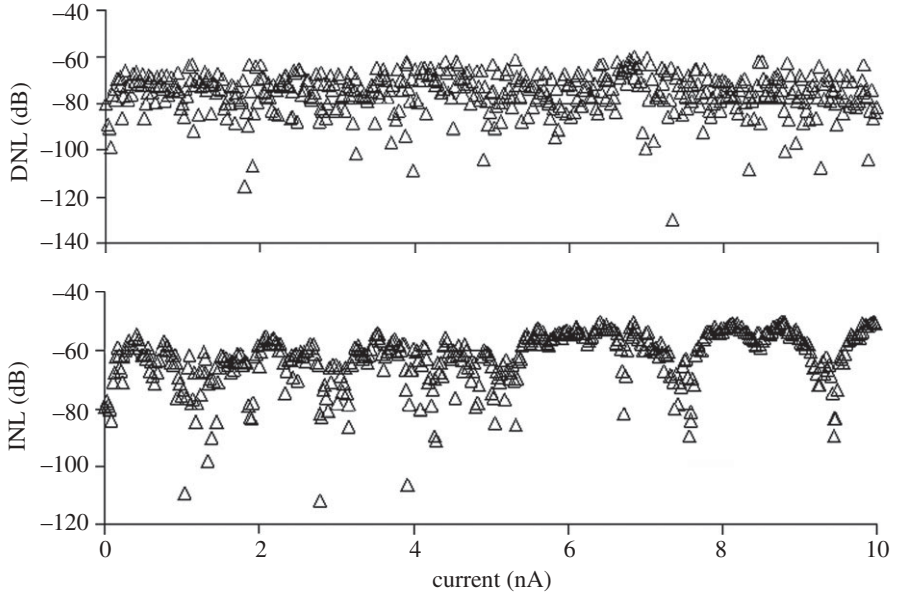

Figure 8. Measured DNL and INL curves of one IRC channel output when the sinusoid input amplitude was swept from 0 to 10 nA. The maximum DNL and INL are 59.8 dB and 50.2 dB, respectively.

A tethered bilayer lipid membrane (tBLM) is useful in functional proteomics research to characterize novel membrane proteins and can be used to develop membrane protein biosensors [4,33]. The equivalent circuit model of a tBLM interface is presented in figure 10, where R_m and C_m represent the resistance and capacitance, respectively, of the lipid bilayer and any embedded proteins, R_S is the solution resistance and C_{dl} is the double layer capacitance [33]. The values of R_m and C_m can be measured to characterize tBLM interface or interrogate any embedded membrane protein-sensing elements.

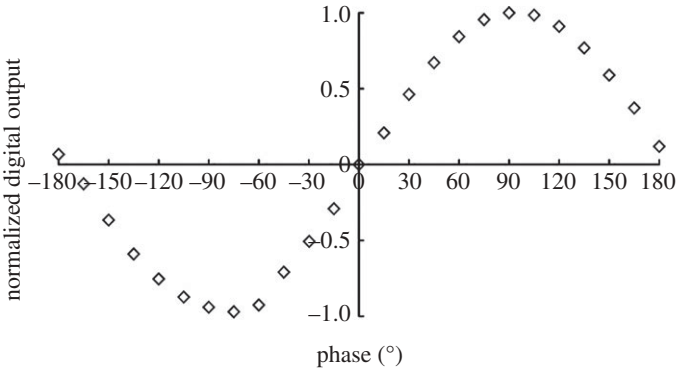

Figure 9. Normalized current response of the IRC chip to a sinusoid input with variable phase and constant amplitude and frequency.

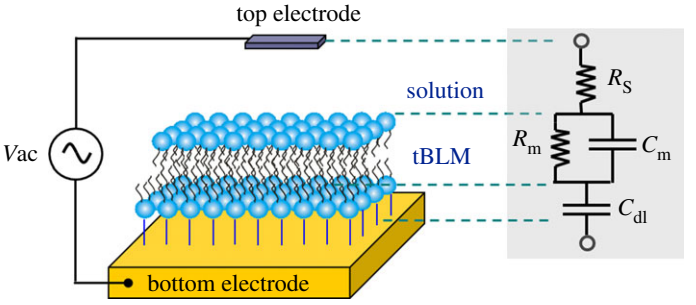

Figure 10. Schematic view and equivalent model of a two-electrode electrochemical site with the bottom electrode coated with a tBLM. In the tBLM equivalent model, R_m and C_m represent the resistance and capacitance of the BLM assembly, respectively, while R_S is the resistance of the solution and C_{dl} describes the double layer capacitance. (Online version in colour.)

Table 1. The performance summary of the IRC.

process	0.5 μm CMOS
power/channel	5.2 μW@3.3 V supply, fclk = 200 KHz
area/channel	0.045 μm^2
resolution	8-bit, 100 fA in the lowest range
frequency range	10 mHz ~ 10 KHz
dynamic range	10 pA–100 nA

To validate the capability of the IRC to measure a real biointerface, an example tBLM was constructed. First, a self-assembled monolayer of 1,2-dipalmitoyl-sn-glycero-3-phosphothioethanol (DPPTE) tether lipid was formed on a clean gold electrode that was patterned on a silicon chip. Then the upper leaflet of the bilayer membrane was deposited by fusion of liposome vesicles made of 1,2-dioleoyl-*sn*-glycero-3-phosphocholine (DOPC) mobile lipids. A data acquisition card (Agilent 6259) was connected to a computer and employed to generate the stimulus sinusoid and collect output data from the IRC, from which the tBLM values of R_m, R_S, and C_m and C_{dl} can be determined. Impedance measurements were conducted with the IRC circuit over the frequency range of 10 mHz to 100 Hz after the tBLM was formed.

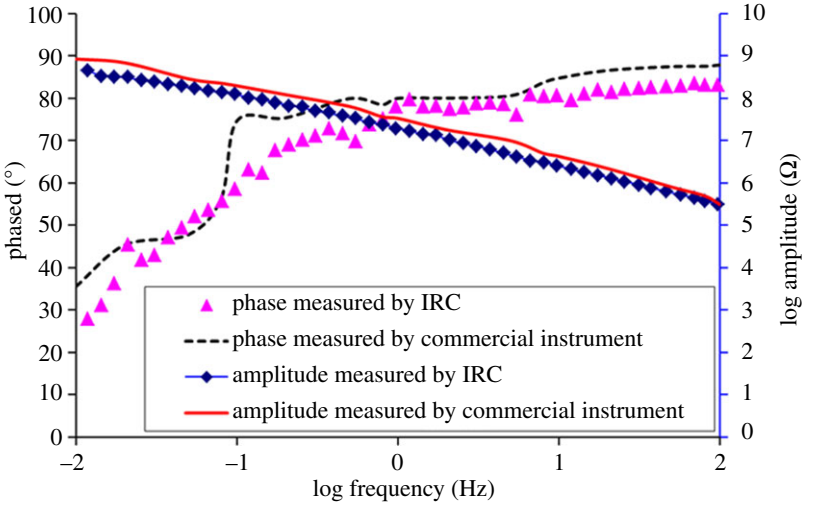

Figure 11. Amplitude and phase after formation of tBLM measured by a commercial instrument (CHI 660 B) and by the IRC over the frequency range 10 mHz–100 Hz. (Online version in colour.)

Figure 11 shows the amplitude and phase data obtained from the IRC as a function of frequency. For comparison, the same biointerface was tested using a commercial impedance instrument (CHI 660 B) and those results are included in figure 11. These data demonstrate that the IRC generates similar results as commercial equipment for extraction of biosensors impedances. The impedance difference between the commercial instrument and IRC measurement results is less than 5% across the frequency spectrum. The *real* and *imaginary* impedance values extracted by the IRC were used to determine the element values of the tBLM equivalent circuit model shown in figure 10. After fitting by ZVIEW software, the normalized values of each component are $R_s = 95\,\Omega$, $R_m = 211 \times 10^3\,\Omega\,cm^{-2}$, $C_m = 0.23\,\mu F\,cm^{-2}$ and $C_{dl} = 2.87\,\mu F\,cm^{-2}$. These values are in good agreement with reported values for tBLM [34]. Using state of the art techniques, BLMs with impedance in the giga-ohm range have been reported [4]. The presented IRC chip can detect impedance up to tens of giga-ohms (more than 1 pA resolution at 10 mV stimulus), which is well beyond the limits of traditional instruments. Thus, the IRC chip enables a new capability to characterize high-quality BLMs using impedance techniques.

6. Conclusion

The design of a fully integrated multi-channel IS chip was described and measurement results from the fabricated 0.5 µm CMOS chip were presented. The chip provides AC stimulus signal generation from 1 mHz to 10 KHz. The impedance-to-digital converter block provides measurement and extraction of *real* and *imaginary* impedance outputs for current inputs, with more than 8-bit resolution in most ranges and a maximum current resolution of 100 fA. Each readout block also digitizes the output and provides serial output through a scan chain of all channels. Each impedance readout channel is compact (0.045 mm^2) and low power (5.2 µW) permitting a single chip to readout a high-throughput array of impedance-based biosensors. Impedance characterization of an example tBLM biointerface was demonstrated. The integration of stimulus and readout functions on a single array chip establishes a powerful platform for biointerface measurement and characterization.

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