Design of a Wideband CMOS Impedance Spectroscopy ASIC Analog Front-End for Multichannel Biosensor Interfaces*

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***Abstract*— This paper presents the preliminary design and simulation of a flexible and programmable analog front-end (AFE) circuit with current and voltage readout capabilities for electric impedance spectroscopy (EIS). The AFE is part of a fully integrated multifrequency EIS platform. The current readout comprises of a transimpedance stage and an automatic gain control (AGC) unit designed to accommodate impedance changes larger than 3 order of magnitude. The AGC is based on a dynamic peak detector that tracks changes in the input current over time and regulates the gain of a programmable gain amplifier in order to optimise the signal-to-noise ratio. The system works up to 1 MHz. The voltage readout consists of a 2 stages of fully differential current-feedback instrumentation amplifier which provide 100 dB of CMRR and a programmable gain up to 20 V/V per stage with a bandwidth in excess of 10MHz.**

I. INTRODUCTION

Recent advances of CMOS technology are leading to the development of complex and miniaturized measurement and analysis platforms for a plethora of biomedical applications, including, DNA and protein analysis [1], [2], cancer detection [3], blood glucose estimation [4] and multitarget biosensing [5], [6]. Electric impedance spectroscopy provides a rapid and accurate method to measure the complex impedance of biological materials such as tissue or analyse chemical reactions occurring at biosensor interfaces. Most commonly EIS is performed by applying a single-frequency current or voltage signal to the biological interface and measuring the phase and magnitude response of the resulting voltage or current, in order to quantify the interface properties. The impedance is measured across a frequency range usually up to 1 MHz. The use of more complex excitation signals, including white noise or a sum of sine waves has the advantage to allow for fast data collection and easier multiplexing among several interfaces.

There is a high demand for the design of complex, flexible, fully programmable and multiplexed EIS integrated platforms for implantable, wearable or biosensor interfaces. Further development is required for the full integration of a number features including fully programmable waveform generators, multiplexing and multifrequency capabilities and configurable readout analog front-ends (AFEs).

The authors are currently developing a flexible EIS platform chip that integrates a programmable waveform generator, a selectable front-end and an integrated digital signal processing unit (DSP). The chip will interface with a set of interdigitated capacitive electrodes to provide impedimetric readout to lateral-flow biosensors for the detection of antibiotic resistant pathogens [7].

The paper is organised as follows. Section II will describe the architecture of the EIS chip and provide detailed explanation on the design of the AFEs. Section III will report simulated results of the performance of the AFEs and Section IV will draw key conclusions and present future developments.

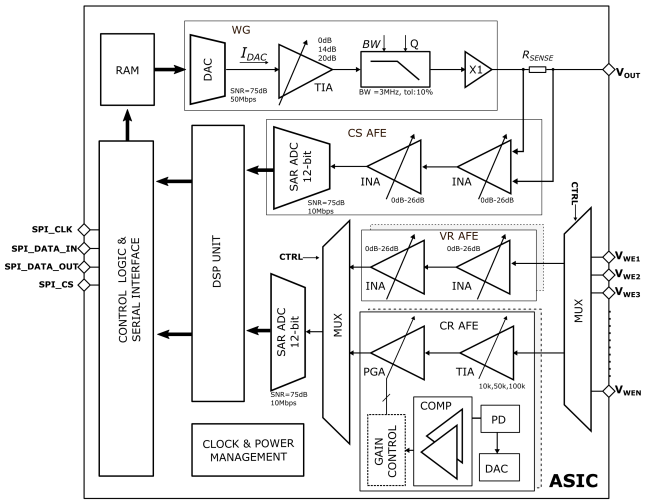

Fig. 1. ASIC architecture.

II. SYSTEM ARCHITECTURE

The architecture of the EIS chip is shown in Figure 1. The waveform generator (WG) comprises of an integrated direct digital synthesizer (DDS), followed by a fully-differential transimpedance amplifier (TIA) and a 3^{rd}-order reconstruction filter. The WG allows to generate sinusoidal excitation signals of frequencies up to 3 MHz and composite signals of up to 5 sinusoids for multifrequency analysis. The amplitude of the signal can be controlled by changing the biasing current of the DAC in order to change its output current amplitude and by varying the TIA gain. Detailed description of the WG is out of the scope of the present paper. The analog front-end (AFE) comprises of 8 voltage readout (VR) channels and 2 current-readout (CR) channels.

An additional current-sensing AFE stage (CS) is used to sense and control the current injection into the V_{OUT}, terminal during operation. The chip also integrates two 12-bit SAR ADCs with a sampling frequency of 10MHz, a DSP unit

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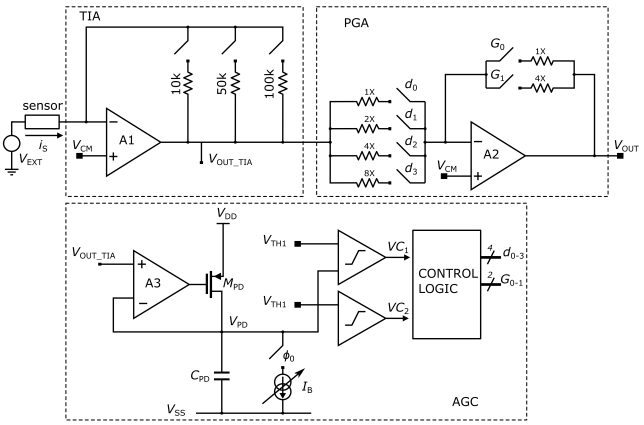


Fig. 2. Architecture of the current-mode channel with automatic gain compensation.

to perform FFT for impedance estimation and control logic and serial interfaces. This paper will focus on the design and performance of the front-end units.

A. Current-readout (CR) AFE

The CR-AFE consists of a TIA input stage followed by a programmable gain amplifier (PGA) stage controlled by an automatic gain control (AGC) unit as shown in Fig. 2. The TIA is implemented by a resistor-feedback opamp configuration. The gain of the TIA is programmable by switching the feedback resistor to 10 kΩ, 50 kΩ or 100 kΩ. The AGC unit tracks the amplitude of the TIA output, $V_{\mathrm{OUT\_TIA}}$, by means of a peak detector.

Amplifier A3 senses the difference between the output of the TIA and the voltage stored by capacitor, C_{PD} and switches on or off transistor M_{PD}, which charges the capacitor to a voltage equal to the peak of the input signal. In order to track a decreasing input signal, however, the peak detector needs a relaxation mechanisms which allows to discharge the capacitor according to the input signal. A switch placed in parallel with the capacitor can be used to reset the capacitor to a known voltage before the peak detector is engaged again. This method, however, is prone to error due to the capacitor time constant and is not suitable for fast signal. One alternative is to bleed a small constant current from the capacitor, although the amount of charge that is removed from the capacitor plate depends on the frequency of the input signal in such way that the amplitude of the current should vary with input frequency. A better solution consists of switching a DC current source placed in parallel with the capacitor at the same frequency as the input signal, as shown in Fig. 2, where the current source I_{B} is implemented by a 4-bit current-steering DAC, to allow for tunability during calibration. The bias current of the DAC is derived by a 1μA β-multiplier followed by a current-divider working in the sub threshold region (not shown).

The output of the peak detector representing the peak value of the input signal is compared to two thresholds, V_{TH1} by and V_{TH1} by 2 latched comparators designed with approximately 40 mV of hysterises. Extensive simulations at different input frequencies resulted in the adopted values of C_{PD}=1pF, I_{B}=300pA, V_{TH1}=0.91V and V_{TH2}=1.01V. The control logic has the function of switching the PGA gain according to the value of the comparator outputs. The use of two threshold values results in three gain ranges (high gain, mid gain and low gain). These ranges can be programmed during device calibration. A resistor-feedback amplifier is used to perform amplification. This allows to achieve large values of gain by simply switching a resistor bank. The amplifier configuration is also shown in Fig. 2. The PGA allows for a coarse gain control by switching control signals G_0 and G_1 for a X1 and a X4 amplification. Fine gain tuning is controlled by switching the input resistor, implemented by a binary-scaled parallel resistor array. The gain of the amplifier is given by:

$$A_{\mathrm{PGA}} = -\frac{R_2}{R_1} = -(G_0 R_{\mathrm{u}} + 4G_1 R_{\mathrm{u}}) \cdot \sum_{n=0}^{3} \frac{d_{\mathrm{n}}}{2^{\mathrm{n}} R_{\mathrm{u}}}, \qquad (1)$$

where R_2 is the feeback resistance, R_1 is the input resistance and R_{u} is the value of the unit resistor of the bank. G_0 and G_1 are mutually exclusive and d_{0-3} cannot be concurrently all zeros. With unit resistors equal to 100 kΩ, the PGA is capable of gains between 1 V/V and 15 V/V and between 4 V/V and 60 V/V. Both opamps *A1* and *A2* are implemented by a 2 stage class AB amplifier with minimum current selector circuit for high drive capability, high swing and efficiency [8]. The amplifier achieves a simulated dc gain of 120dB, a unity gain bandwidth of approximately 34 MHz with a phase margin of 60° and consumes 105 μA. The simulated input-referred noise is 98 nV/$\sqrt{Hz}$ at 10 kHz and 35 nV/$\sqrt{Hz}$ at 100 kHz.

B. Voltage-readout (VR) AFE

The VR AFE consists of 2 stages of variable gain instrumentation amplifiers (INA). Each INA is based on a current feedback architecture [9]. The architecture of the INA is shown in Fig. 3. The input pair M_1 and M_2 are degenerated by a source resistor R_{S}, giving raise to an ac current equal to the ratio between the input voltage and the sum of the source resistance of the input pair ($= 1/gm$) and R_{S}.

The current is conveyed to the output by the diode load transistors M_3 and M_4, where it is amplified by a factor of 1 (*SW*1) or 5 (*SW*2) by switched current mirrors M_6-M_7 and M_8-M_9. The overall amplifier gain is then proportional to the ratio between the load resistor R_{L} and R_{S}. By switching R_{S}, instead of R_{L} the amplifier gain can be varied without greatly affecting its bandwidth. Series degeneration results also in improved linearity as compared to shunt degeneration often adopted in similar configurations. The series resistor R_{S} is implemented by a 3-bit resistor bank, shown in the inset of Fig. 3. R_{L} is set to 2.1kΩ, whereas the unit resistor of the bank is set to 3.5kΩ. Extensive simulations were performed to optimised the sizing of the resistor bank to obtain accurate gain values. A common-mode feedback (CMFB) circuit was implemented (not shown) in order to stabilise the output common mode voltage to mid-rail (0.9V). This is based on

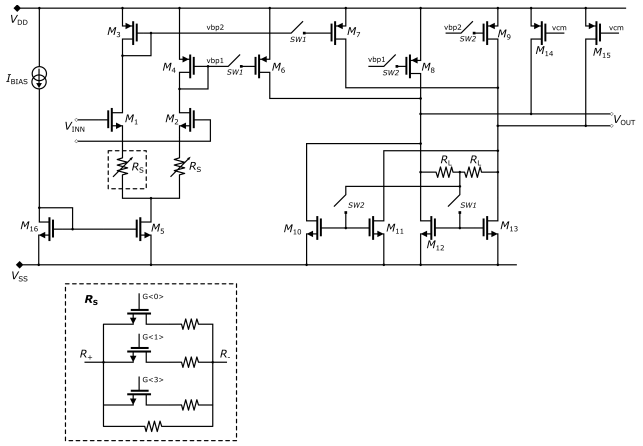


Fig. 3. Schematic of the fully differential programmable INA.

a difference-differential amplifier that senses the differential output and injects common-mode current to the amplifier output via current sources M_{14} and M_{15}. The sink transistors M_{10}-M_{13} are scaled to draw a larger current than the source transistors in order to make the CMFB effective. The sink transistors are also switched depending on the output current settings $SW1$ and $SW2$ is order to save power when the low gain setting is selected. The INA is biased with a tail current source of 120 μA, resulting in the input pair source resistance, $1/g_m$, of 700 Ω. The output current through each branch is switched between 60μA and 300 μA. The on-resistance of the switches was designed to be in the order of 20 Ω, a factor of 10 smaller than the smaller value of R_S, which is set to 200 Ω.

III. Simulated Performance

The circuits were designed in a 6-metal 0.18μm CMOS technology with a supply voltage of 1.8V. The circuits were simulated using Cadence Virtuoso.

A. TIA

The simulated performance of the complete current read-out front-end is reported in this section. The performance of the class-AB opamps was summarised in the previous section. The simulated range of PGA gain is shown in Fig. 4 for the two settings G_0 and G_0. When G_0 is selected the simulated gain ranges versus d code is between 1 V/V and 14.66 V/V with a nominal maximum error of 2.2% at a typical corner. When G_1 is selected the gain ranges between 3.98 V/V and 58.4 V/V with a nominal maximum deviation of 2.2% at a typical corner.

The correct performance of the AGC was assessed by performing transient analysis with a small sinusoidal input signal varying in amplitude over time. The PGA gain were set to 40 V/V, 5 V/V and 2 V/V for the 3 cases where the input signal amplitude is below, between or above the comparator thresholds. Fig. 5 shows the relation between the input signal, the output of the peak detector and the output of the PGA. At start up C_{PD} is charge to mid-rail potential (0.9V) and both comparator outputs a low. The

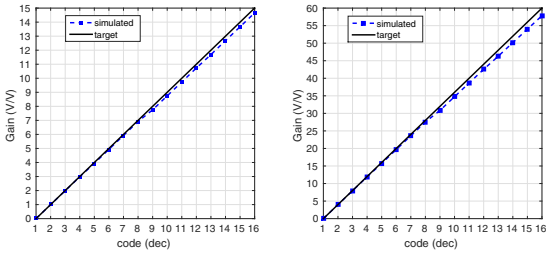


Fig. 4. Range of simulated gains of the PGA for different code settings.

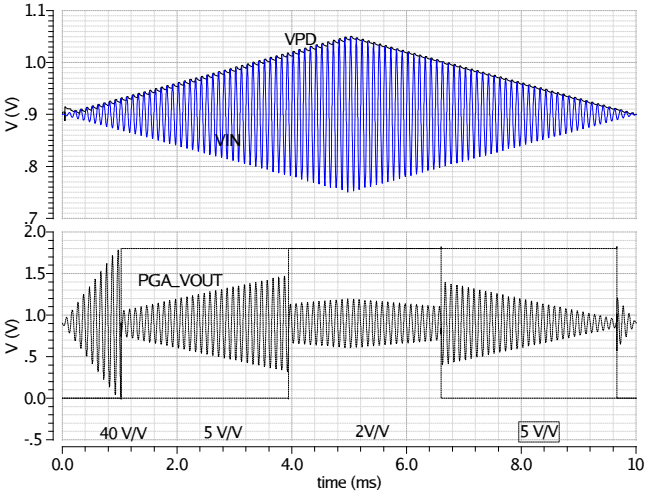


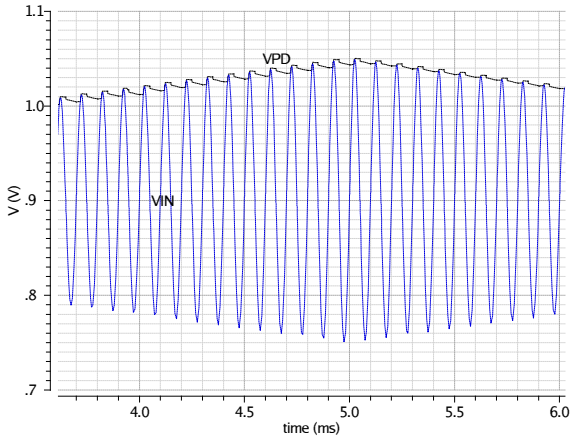
Fig. 5. Transient simulation of the AGC unit at 10 kHz. The amplitude of the input signal varies between 100μVpp and 150 mVpp.

PGA gain is set to its high range. As VIN increases, V_{TH1} is crossed and AGC unit reduces the PGA gain to the mid range. As V_{TH2} is crossed the PGA gain is switched to the lowest setting. Fig. 5 also shows the correct performance of the switched current source in bleeding sufficient current to allow the peak detector to keep tracking the input signal when this is decreasing. The PGA gain is correctly changes once the thresholds are crossed again. The visible asymmetry in the timing of the switching is due to the hysterises in the comparators. These are fundamental as the output of the peak detector varies by few mV within one cycle, which may cause the comparators to erroneously toggle.

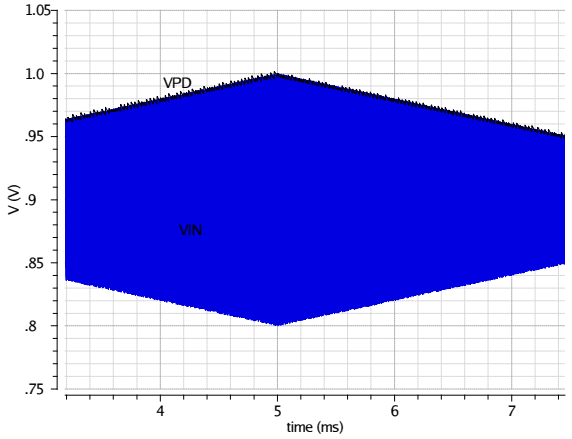
A more detailed representation of the tracking capability of the peak detector is shown for different input frequencies in Fig. 6. The simulated performance of the AGC was successfully tested for frequencies between 1 kHz and 1 MHz. Results are not shown here for practical reasons.

B. INA

Fig. 7 shows the simulated gain of the INA for different ratios of R_L and R_S, and different output current settings. The gain can be varied between 1 V/V and 4 V/V (0 dB-12 dB) and between 5V/V and 20 V/V (14 dB - 26dB). Gains up to 400 V/V are achieved by cascading 2 INA stages. The bandwidth of the amplifier is approximately constant and equals 26 MHz for the SW1 setting and 11.5 MHz for the SW2 setting. The total current consumption of each stages



(a) 10 kHz



(b) 100 kHz

Fig. 6. Transient simulation of phase detector at different frequency. I_B was set to 300pA and switched at the frequency of the input signal.

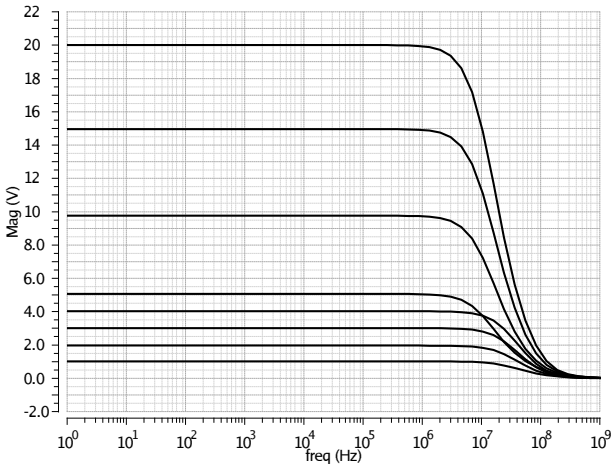
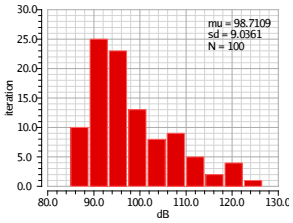
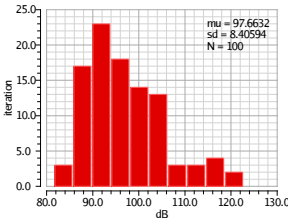


Fig. 7. Simulated gain of a single stage of the INA for different output current settings



(a) SW1



(b) SW2

Fig. 8. Simulated Monte Carlo analysis of effects of process variations and mismatches on the INA CMRR. Monte Carlo analysis was performed on 100 runs using 3-σ models

is approximately 280 μA for the low gain setting, $SW1$ and 690 μA for the high gain setting, $SW2$.

The CMRR of the amplifier was simulated for a typical corner across process variations and component mismatches by performing 100 runs of Monte Carlo analysis. This resulted in a mean CMRR in the order of 100 dB as reported in Fig. 8. The simulated input-referred noise is 86 nV/$\sqrt{Hz}$ at 10 kHz and 35.2 nV/$\sqrt{Hz}$ at 100 kHz. Transistors M_1-M_2 are the major contributors of the overall noise.

IV. CONCLUSIONS

This paper has presented the design and simulation results of a multichannel current and voltage readout AFE, which is part of a flexible multifrequency fully integrated EIS system. This development addresses the need for smart, flexible and portable analytical tools for a range of biological interfaces including tissue and biosensors, for a number of sensing applications including cancer detection, body fluid analysis and immunosensor interfaces.

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