A 0.18 μm Biosensor Front-End Based on $1/f$ Noise, Distortion Cancelation and Chopper Stabilization Techniques

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***Abstract*—This paper presents a novel sensor front-end circuit that addresses the issues of $1/f$ noise and distortion in a unique way by using canceling techniques. The proposed front-end is a fully differential transimpedance amplifier (TIA) targeted for current mode electrochemical biosensing applications. In this paper, we discuss the architecture of this canceling based front-end and the optimization methods followed for achieving low noise, low distortion performance at minimum current consumption are presented. To validate the employed canceling based front-end, it has been realized in a 0.18 μm CMOS process and the characterization results are presented. The front-end has also been tested as part of a complete wireless sensing system and the cyclic voltammetry (CV) test results from electrochemical sensors are provided. Overall current consumption in the front-end is 50 μA while operating on a 1.8 V supply.**

***Index Terms*—1/f noise, chopping, current mode electrochemical biosensor, distortion canceling, low noise, low power, noise canceling, strong inversion, transimpedance front-end (read-out), weak inversion.**

I. Introduction

FRONT-ENDS used in current mode biosensing applications [1]–[6] are typically required to detect signals with a wide dynamic range (DR) which normally extends from as low as pA's to μA's or more. In order to detect such signals with low current levels, 1/f noise is the main limiting factor and this is usually rejected using conventional techniques [7] like auto-zeroing, which has been previously applied [8], [9] to biosensor front-ends and chopper stabilization, which has been widely applied to voltage mode sensor front-ends like ECG, EEG based signal acquisition systems [10], [11] and many other low frequency sensor applications [12].

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But in addition to the above 1/f noise limitation, there is also the limitation of distortion in the front-end. Here distortion assumes significance mainly because of the wide DR, the direct trade-off between current consumption-distortion arising from the current mode nature of the inputs and the linearity required being 1% or less typically. But as before, distortion is also minimized and common techniques like negative feedback [8] and log domain compression [13] have been employed previously.

However in addition to the above mentioned techniques, there is also the technique of canceling which can be used to reject both of them simultaneously [14]. The canceling technique for minimizing front-end non-idealities has been introduced as recently as 2001 [15] and it has been previously applied to wideband LNA's in [16], [17] for canceling the input stage thermal noise (partially) and distortion.

The current work is based on this canceling technique where it has been taken advantage of to minimize both 1/f noise and distortion, and eventually a low power biosensor front-end is realized employing canceling techniques. The front-end thus realized is targeted for a personalized patient treatment system employing electrochemical sensors for biomolecule detection but it can also be applied to other current mode sensing applications. In this paper, this canceling based front-end circuit is presented in detail and is organized as follows. In Sections II–VI, a detailed description of the individual blocks in the front-end namely the common gate TIA, the noise canceling TIA, the noise canceling chopper stabilized (NCCS) [14] amplifier and the capacitively coupled (CC) amplifier are presented. Later in Section VII, the circuit design details are given followed by a discussion of the measurements results. Finally in Section VIII, a comparison of achieved performance with the other existing works is provided and conclusions are drawn.

II. Common Gate (CG) TIA

Among the current mode input front-ends, the simplest one is the CG stage to which the canceling technique is applied in this work. Nevertheless it needs to be mentioned that this technique is not limited to the CG stage alone but it can be applied to other circuit topologies as well including opamp based front-ends [15], [16]. The intent of this work however is not to go into the individual details of each of them but to use the CG stage and apply canceling to see how $1/f$ noise and distortion can be minimized.

The schematic of the CG stage along with its small signal model is shown in Fig. 1. From Fig. 1(b), assuming the gate and

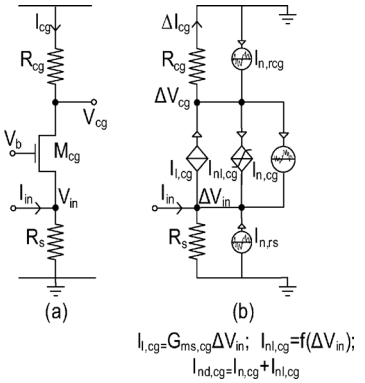

Fig. 1. (a) CG TIA. (b) Model of CG TIA.

the bulk potentials of M_{cg} are constant, the instantaneous output voltage for an input current I_{in} is given by

$$\Delta V_{cg} = (I_{l,cg} + I_{nl,cg})R_{cg} \tag{1}$$

where $I_{l,cg}$ and $I_{nl,cg}$ refer to the linear and the non-linear (distortion) currents respectively. In (1), we have ignored the noise contributions for the sake of simplicity but they are included later. The above two factors $I_{l,cg}$ and $I_{nl,cg}$ can be derived analytically using the ideal MOS $\mathrm{Id} - \mathrm{Vgs}$ equation whose derivation is given in appendix A. Accordingly ΔV_{cg} can be rewritten as

$$\Delta V_{cg} = (\alpha_1 I_{in} - \alpha_2 I_{in}^2)R_{cg} \tag{2}$$

where $\alpha_1 = k_{deg}/(k_{deg}+1)$, $\alpha_2 = 1/(2I_{cg}k_{deg})$ for M_{cg} in weak inversion (WI) (reason for WI biasing given below) and the factor $k_{deg} = G_{ms,cg}R_s$ is the degeneration factor with $G_{ms,cg} = I_{cg}/U_T$ being the source transconductance. For most practical cases, $k_{deg} \gg 1$ and hence $\alpha_1 \approx 1$. From (2), the transimpedance $R_{m,cg}$ is given by

$$R_{m,cg} = \frac{|\Delta V_{cg}|}{|I_{in}|} = \alpha_1 R_{cg} \approx R_{cg}. \tag{3}$$

Note that this transimpedance factor $R_{m,cg}$ can also be derived directly from Fig. 1(b) in a straightforward manner knowing that the input impedance $R_{in} = R_s/(1+k_{deg})$ which then leads to $I_{l,cg} = (G_{ms,cg}R_{in})I_{in} = \alpha_1 I_{in}$ and hence $R_{m,cg} = \alpha_1 R_{cg} \approx R_{cg}$.

Harmonic distortion of the CG stage can also be derived from (2) which is given by

$$HD_{2,cg} = \frac{|\alpha_2|}{2|\alpha_1|} I_{in} \approx \frac{I_{in}}{4I_{cg}k_{deg}} \tag{4}$$

where one can see distortion being inversely related to the bias current I_{cg} at a constant k_{deg} thereby implying a current-distortion trade-off. Accordingly, if M_{cg} were to be biased in weak inversion (WI), the required bias current will be lower than in strong inversion (SI) because of the higher current efficiency (G_m/I ratio) but with the penalty of higher distortion. Similarly the contrary is true for SI biasing of M_{cg}. The result of this trade-off is distortion limits the minimum achievable current consumption in the CG stage. Here in this work, this trade-off is relaxed by using canceling technique such that M_{cg} can be biased in WI itself for low power consumption as explained in the next section.

Next considering the noise contributions alone, the input (I/P) referred current noise power spectral density (PSD) is given by

$$\begin{aligned} S_{n,cg} &= \frac{4kT}{R_{m,cg}^2}\left(R_{cg} + \frac{R_{cg}^2}{R_s} + \frac{\gamma G_{m,cg}R_{cg}^2}{(1+k_{deg})^2}\left[1+\frac{f_{k,cg}}{|f|}\right]\right) \\ &= \frac{4kT}{\alpha_1^2 R_{cg}}\left(1 + \frac{R_{cg}}{R_s} + \frac{\gamma G_{m,cg}R_{cg}}{(1+k_{deg})^2}\left[1+\frac{f_{k,cg}}{|f|}\right]\right) \\ &= \frac{4kT}{\alpha_1^2 R_{cg}}\gamma_{cg} \end{aligned} \tag{5}$$

where $\gamma \approx n.\delta$ with $\delta \approx 1/2$ for M_{cg} in WI, $f_{k,cg}$ being the corner frequency of M_{cg} and γ_{cg} being the total excess noise factor [14]. The dominant noise term in (5) is that of the $1/f$ noise of M_{cg} even in the presence of degeneration and it is also the main factor that limits the sensitivity of the CG stage. This limitation is overcome in this work in the same way as distortion by way of using the canceling technique and $1/f$ noise of M_{cg} (along with its thermal noise) is also rejected.

Hence neglecting the noise contribution (both thermal and $1/f$) of M_{cg} for the above reason, the resulting I/P noise PSD is given by

$$S_{n,cg,in} = \frac{4kT}{\alpha_1^2 R_{cg}}\gamma_{cg} \approx \frac{4kT}{R_{cg}}\left(1 + \frac{R_{cg}}{R_s}\right) \tag{6}$$

where $\alpha_1 \approx 1$ is assumed and $\gamma_{cg} = (1 + R_{cg}/R_s)$. From (6), the I/P noise without the noise of M_{cg} is limited by thermal noise of R_{cg}, R_s (thankfully they do not ideally generate $1/f$ noise) whose resistance values are restricted by the voltage headroom constraints for a given I_{cg}. This constraint also implies if M_{cg} were to be biased in WI, then the lower current level will provide the additional freedom to maximize R_{cg}, R_s resulting in lower input noise. This is an added advantage of WI biasing in the CG stage.

III. Noise Canceling TIA (CG-CS Stage)

The noise canceling TIA (shown in Fig. 2) which is based on the noise canceling LNA of [17] is nothing but a CG TIA with an auxiliary common source (CS) stage added in parallel. The addition of the CS stage helps to cancel the non-idealities of the input stage M_{cg} under certain matching conditions.

The matching condition for cancelation can be derived from the instantaneous output voltage which is given by

$$\begin{aligned} \Delta V_{cgcs} &= \Delta V_{cg} - \Delta V_{cs} \\ &= (I_{in} + I_{n,rs})\left[\frac{R_{cg}k_{deg} + G_{m,cs}R_{cs}R_s}{k_{deg}+1}\right] + I_{n,rcg}R_{cg} \\ &\quad - I_{nd,cg}[R_{cg} - G_{m,cs}R_{cs}R_s] + (I_{n,rcs} + I_{nd,cs})R_{cs}. \end{aligned}$$

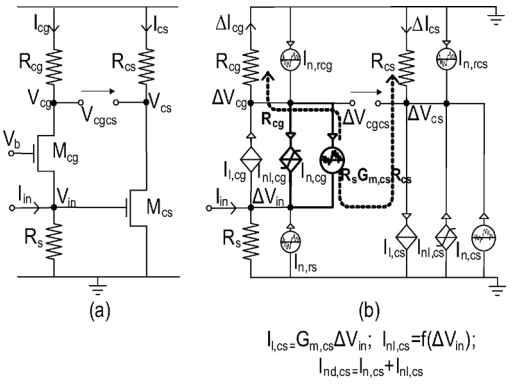

Fig. 2. (a) Noise canceling TIA. (b) Model of noise canceling TIA.

(7)

In (7), if the condition $R_{cg} = G_{m,cs}R_{cs}R_s$ or equivalently

$$\frac{R_{cg}}{R_s} = G_{m,cs}R_{cs} \tag{8}$$

gets satisfied, then the effective gain (transfer function) for the non-ideal current $I_{nd,cg}$ gets nulled as seen from (7) and this property can be used to reject noise ($1/f$ and thermal), distortion of M_{cg}. Under the above matched condition, the CG transistor M_{cg} behaves as a transconductor which is ideally noise-less and distortion-less but still detecting input currents.

However even if M_{cg} behaves ideally, the CS stage is still non-ideal which adds noise and distortion [given by $I_{nd,cs}$ in Fig. 2(b)] that do not get canceled. Now in order for the canceling stage to be advantageous over a CG stage alone, these nonidealities also need to be minimized eventually without sacrificing greatly on power consumption which is discussed next.

Under the canceling condition, the instantaneous output voltage ΔV_{cgcs} reduces to

$$\Delta V_{cgcs} = I_{in}R_{cg} + (I_{n,rs} + I_{n,rcg})R_{cg} + (I_{n,rcs} + I_{nd,cs})R_{cs}. \tag{9}$$

The transimpedance $R_{m,cgcs}$ from (9) is given by

$$R_{m,cgcs} = \frac{|\Delta V_{cgcs}|}{|I_{in}|} = R_{cg} \tag{10}$$

which is higher by a small factor $(k_{deg}+1)/k_{deg}$ than $R_{m,cg}$. This is because the auxiliary CS stage gain is constructive for the signal I_{in} but destructive for the non-idealities $I_{nd,cg}$.

From (9) the non-linear output of the canceling stage ignoring the noise contributions is given by (derivation given in appendix B)

$$\Delta V_{cgcs} = (\theta_1 I_{in} + \theta_2 I_{in}^2)R_{cg} \tag{11}$$

where $\theta_1 = 1$ and $\theta_2 = U_T/(2I_{cg}[V_{g,cs} - V_{T0}]k_{deg})$ with U_T being the thermal voltage. Here M_{cs} is biased in SI and the consequence of this is shown later while comparing the distortion coefficients between the two stages. The harmonic distortion of the canceling stage as derived from (11) is given by

$$HD_{2,cgcs} = \frac{|\theta_2|}{2|\theta_1|}I_{in} \approx \frac{I_{in}}{4I_{cg}k_{deg}}\frac{U_T}{V_{g,cs} - V_{T0}} \tag{12}$$

which is similar to (4) except for the factor $U_T/(V_{g,cs} - V_{T0})$.

Considering next the noise contributions, we see from (9) while the noise of M_{cg} is canceled under the matching condition, the noise due to R_{cg}, R_s are not canceled and moreover there is the additional noise coming from the CS stage. Including only the noise sources that remain subsequent to canceling, the I/P noise PSD of the canceling stage is given by

$$S_{n,cgcs,in} = \frac{4kT}{R_{cg}}\left(1 + \frac{R_{cg}}{R_s} + \frac{\gamma\frac{R_{cg}}{R_s}+1}{G_{m,cs}R_s} + \frac{\gamma R_{cg}}{G_{m,cs}R_s^2}\frac{f_{k,cs}}{|f|}\right) \tag{13}$$

where $\gamma \approx n.\delta$ with $\delta \approx 2/3$ for M_{cs} in SI, $f_{k,cs}$ being the corner frequency of M_{cs}. Comparing (5) and (13), it is obvious that $1/f$ noise of M_{cg} is now replaced by $1/f$ noise of M_{cs} which is equally dominant. But then this $1/f$ noise is not a major concern as it can be removed by chopping the CS stage as explained in Section VI below. Hence under the assumption of chopping for the CS stage, its $1/f$ noise can therefore be neglected and the I/P noise PSD in (13) reduces to

$$S_{n,cgcs,in} = \frac{4kT}{R_{cg}}\left(\gamma_{cg} + \frac{\gamma\frac{R_{cg}}{R_s}+1}{G_{m,cs}R_s}\right) = 4kT\frac{\gamma_{cgcs}}{R_{cg}} \tag{14}$$

where γ_{cgcs} is the excess noise factor of the canceling stage.

IV. Noise-Distortion Comparison

From the above derived excess noise factors and distortion coefficients for both the CG and the CG-CS stages, a noise-distortion comparison in relation to the current consumption is carried out next. The conditions chosen for the comparison between the two stages are such that the CG parameters R_{cg} and I_{cg} are identical in both the stages while M_{cg} is assumed to be in WI (for reasons mentioned in Section II). $V_{g,cs} - V_{T0}$ is swept by varying R_s and R_{cs} is chosen such that the canceling condition given by (8) is always satisfied. Since the current I_{cg} is chosen to be identical in both the stages, the CS stage consumes additional current I_{cs} whose magnitude in relation to I_{cg} is chosen optimally from the below noise comparison.

A. Distortion

Using the distortion coefficients given in (4) and (12), relative distortion between the two stages is calculated as

$$D = \frac{HD_{2,cgcs}}{HD_{2,cg}} = \frac{U_T}{V_{g,cs} - V_{T0}}. \tag{15}$$

For a large $V_{g,cs} - V_{T0}$ (or equivalently M_{cs} in SI), $D \ll 1$ and the canceling stage generates lower distortion than the CG stage alone. In Fig. 3, the factor D is plotted as a function of $V_{g,cs} - V_{T0}$ along with the overall THD ratio as calculated from

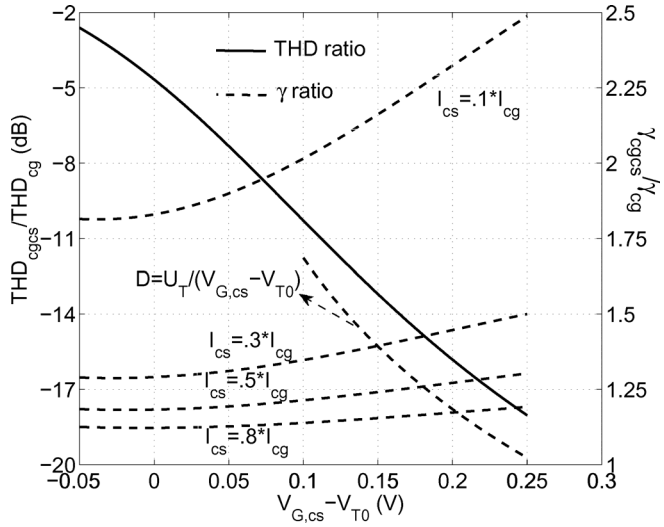

Fig. 3. Noise-Linearity comparison of the CG and the CGCS stages showing the effect of decreasing distortion in the CGCS stage for increasing $V_{G,cs}-V_{T0}$ and the excess thermal noise, the excess current required for achieving it. The graph is plotted for values of $R_{cg} = 60\ \mathrm{k}\Omega$, $I_{cg} = 17\ \mu\mathrm{A}$.

the continuous WI-SI ideal MOS equation $I_{ds} = I_{spec}.[ln(1 + e^{v})]^2$ [19]. As evident from both the plots, for M_{cs} in SI, the factor of reduction in distortion is significantly lower which is proportional to $V_{g,cs} - V_{T0}$ whereas for M_{cs} closer to WI, it gradually decreases and eventually becomes negligible since its distortion is now nearly the same as that of the independent CG stage in WI.

B. Noise

For noise comparison, the excess noise factors γ_{cg}, γ_{cgcs} are used and their ratio $\gamma_{cgcs}/\gamma_{cg}$ is plotted in Fig. 3 [1] for different values of I_{cs}. From this plot, the current I_{cs} required to minimize the excess thermal noise is chosen.

From the plot, for $I_{cs} \approx I_{cg}$, it can be seen that the excess noise is nearly negligible but the overall current consumption in the canceling stage is nearly twice compared to the CG stage alone. On the other hand, for $I_{cs} \ll I_{cg}$, the current overhead is now negligible but the excess thermal noise is significant. Alternatively in the region $I_{cs} \leq .5I_{cg}$, it can be seen that the excess noise is only slightly higher and also the excess current is only 50% more or less. The above observation leads to the conclusion that, choosing $I_{cs} \approx 0.5I_{cg}$ is sufficient and also optimal for the canceling stage which ensures both the excess noise and the excess current are only marginally higher.

The overall conclusion of the above noise-distortion comparison is, a CG-CS stage under the matched cancelation condition and WI-SI biasing respectively achieves a lower distortion compared to an independent CG stage in WI. Particularly the distortion level in the CG-CS stage is lower by a factor nearly $(V_{g,cs} - V_{T0})/U_T$ (without considering second order effects) while the excess current and the excess noise are only marginally higher (50% more or less). This improvement can also be viewed alternatively as, the current consumption required in a CG-CS stage for the same distortion performance is only lower in relation to an CG stage (from (4) and (12) for a constant k_{deg}). Hence a CG-CS stage is either capable of achieving a lower distortion performance or a lower current consumption in relation to an CG stage thanks to both the distortion cancelation property inherent to the canceling technique and the employed WI-SI biasing method. Between the two, distortion canceling is responsible for decoupling the current consumption-distortion requirement and relaxing the current-distortion trade-off while the WI-SI biasing is responsible for achieving an improved performance.

By virtue of the above relative advantage of the noise canceling TIA over a CG TIA, the former is used as the first gain stage of the biosensor front-end in this work. Here it needs to be mentioned further that this advantage not only holds for the canceling stage alone but also holds good even after the CS stage is chopped in order to remove its $1/f$ noise. With this chopping included, the canceling stage will then have the added advantage of lower noise too compared to the CG stage.

V. Robustness of Canceling

In the analysis done above for the canceling TIA, it was assumed that the canceling condition is satisfied ideally ($R_{cg}/R_s = G_{m,cs}R_{cs}$) and the impact of parameter variations were neglected. But in practice, the canceling accuracy will be limited by the degree to which the canceling condition ($R_{cg}/R_s = G_{m,cs}R_{cs}$) is satisfied which in turn depends on process and temperature variations. In order to control the parameter variations due to variations in process, temperature etc., and ensure a certain degree of cancelation, a suitable biasing circuitry will be needed which is discussed next.

The biasing circuitry for the canceling stage is shown in Fig. 4. From a PTAT reference current I_{ref}, V_b is first generated by using a stack of diode connected transistors M_1 and M_2 with M_1 mirroring M_{cg} and M_2 mirroring M_{cs} respectively. The bias V_b sets the current I_{cg} in the CG stage in such a way that $V_{g,cs} - V_{T0}$ is held nearly constant and the current I_{cs} always mirrors I_{ref}. Since I_{cs} always mirrors I_{ref}, this implies $G_{m,cs}$ is nearly constant for a constant PTAT reference I_{ref}. Note that any parameter variations in R_s do not greatly impact I_{cs} thanks to the feedback effect and the resistor degeneration which ensure $V_{g,cs} = I_{cg}R_s$ remains nearly constant. Now for a given current I_{cs}, the replica CS stage generates the required bias voltage V_{rcs} for M_{rcs} to be biased in the linear region. Implementing R_{cs} as shown using a linear region MOS ensures R_{cs} tracks process and temperature variations and also gives the additional flexibility in terms of tuning if needed.

Apart from controlling the parameter variations in $G_{m,cs}$ and R_{cs}, variations in R_{cg} and R_s also need to be controlled. But this can be easily achieved by choosing the same unit resistance for both of them which ensures the ratio R_{cg}/R_s remains constant always.

The achievable rejection in the canceling stage with this biasing circuitry is evaluated using Monte Carlo simulations and

[1] While evaluating γ_{cg} and γ_{cgcs}, only the thermal noise contributions are included as we are mainly interested in optimizing the excess thermal noise-excess current in the canceling stage for now. Effect of $1/f$ noise of M_{cs} is considered separately in Section VI.

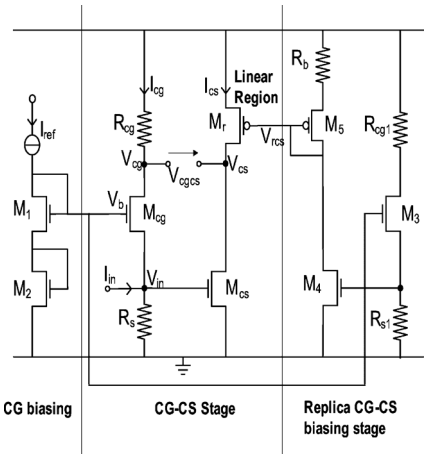

Fig. 4. Schematic of canceling stage with biasing circuitry.

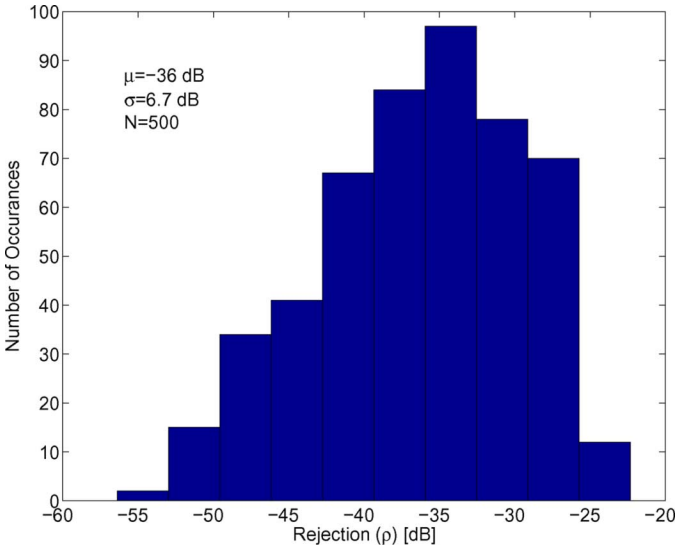

Fig. 5. Achievable rejection in the canceling stage evaluated using Monte Carlo simulations for the circuit shown in Fig. 4.

the results are shown in Fig. 5. The rejection factor for the CG non-idealities is calculated in Fig. 5 as

$$\rho = \frac{\Delta V_{cgcs}}{\Delta V_{cg}}. \tag{16}$$

From Fig. 5, we see that for 1σ deviation, the rejection is nearly -30 dB and the worst case rejection is nearly -20 dB. To have an idea of whether this rejection is sufficient or not, a condition for the minimum required rejection performance needs to be defined which is given below for both $1/f$ noise and distortion. For $1/f$ noise reduction, the minimum required rejection is given by the condition that the required corner frequency of the canceling stage subsequent to canceling (f_k') (here again we neglect the $1/f$ noise effects of M_{cs} temporarily) is less than the corner frequency of the CG stage alone f_k. Equivalently, this can be expressed as $\rho < f_k'/f_k$. Similarly for the case of distortion, the minimum required rejection is given by the condition that the harmonic distortion of the CG stage subsequent to cancelation ($\rho HD_{2,cg}$) has to be less than the harmonic distortion of the CS stage $HD_{2,cgcs}$. Equivalently, this can be expressed as $\rho < D$.

As a numerical example, if we consider a $V_{g,cs} - V_{T0} = 200\,\mathrm{mV}$ sufficient to keep M_{cs} in SI, then the factor D as given by (15) is -18 dB. This implies the minimum required rejection performance in the canceling stage has to be less than -18 dB for the distortion of the CG stage to remain negligible and for the eventual distortion to be solely determined by the CS stage alone. From Fig. 5, for 1σ variation, the rejection is well below the limit and it easily satisfies the requirement condition. If 3σ variation is considered, we can see the rejection ρ is a bit more than D and as a result the overall THD will be approximately 3 dB higher. Although the overall THD increases for the 3σ condition, this amount of rejection is however sufficient as the overall distortion is anyway lower compared to the CG distortion by nearly 15 dB.

Hence, by using a biasing circuitry as proposed or by using other suitable biasing schemes, the effectiveness of the cancelation technique can be ensured even for process, temperature variations. In such a case, the achievable rejection is eventually limited only by matching.

VI. Sensor Front-End

In [14], a front-end utilizing the canceling stage was presented but it was limited to only the first gain stage. Below we improve upon the circuit presented in [14] and a complete two stage sensor front-end architecture based on canceling techniques is presented.

A. Noise Canceling Chopper Stabilized (NCCS) Amplifier

In the noise analysis done previously for the canceling stage, the effect of $1/f$ noise of the CS stage was not considered for the sake of simplicity. However this $1/f$ noise is as dominant as the $1/f$ noise of M_{cg} and in its presence, the canceling stage used independently is no better than the CG stage alone. To overcome this limitation, the CS stage is chopped as shown in Fig. 6 (biasing not included) which then ensures its $1/f$ noise is also rejected apart from $1/f$ noise of M_{cg} that gets rejected by canceling. The resulting noise performance is then limited mainly by thermal noise alone with the input noise PSD under the matched condition given by

$$S_{n,nccs} = \frac{8kT}{R_{cg}}\left(\gamma_{cgcs} + .8525\frac{f_{k,cs}}{f_{chop}}\frac{\gamma R_{cg}}{G_{m,cs}R_s^2}\right) \tag{17}$$

where f_{chop} is the chopping frequency. For $f_{k,cs} < f_{chop}$, only the residual $1/f$ noise of the CS stage remains as given by the second term in the above equation which is only negligible in comparison to other factors.

The above topology which uses a combination of the canceling and the chopping techniques to reject the different $1/f$ noise sources is referred as the NCCS amplifier. It is basically a pseudo-differential version of the canceling stage with two identical CG-CS stages but with the the addition of chopping to the CS stage. This NCCS stage is similar to the chopper stabilized CG TIA in the fact that both reject $1/f$ noise and achieve low noise performance. But then the difference is although the chopped CG TIA offers low noise performance, it however does

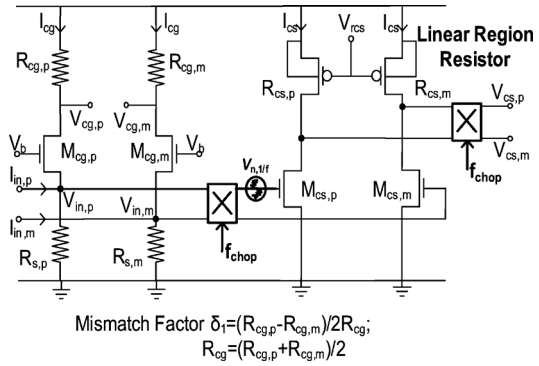

Fig. 6. Schematic of NCCS transimpedance amplifier.

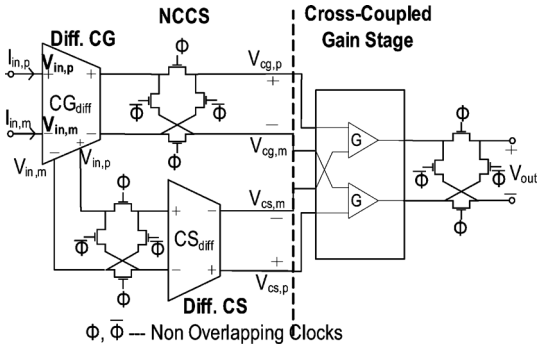

Fig. 7. Block diagram of the NCCS amplifier along with the second gain stage. (Dechopping of the NCCS outputs is shifted to the output of the second gain stage for low frequency noise rejection in the second stage.)

not have the combined low power-low distortion advantage of the NCCS amplifier and further its minimum achievable input impedance (R_{in}) is limited by the chopper switch resistances. In the NCCS amplifier, this is however not the case since the chopper switches are only present at the CS inputs and hence do not greatly impact R_{in}.

B. Capacitively Coupled (CC) Amplifier

Before feeding the outputs of the NCCS amplifier to the sensor interface back-end stages like the A/D converter, a second stage is required for additional gain and also to perform the difference operation in order to complete the canceling. In Fig. 7 which is a simplified block diagram of the two stage front-end, the second stage connected in a cross-coupled configuration is shown. In the current work, this second stage is implemented using a capacitively coupled amplifier [20] (schematic shown in Fig. 8) which gives better canceling accuracy by virtue of its good gain matching characteristics. A resistive feedback gain stage is also a suitable option here for the second gain stage but then it was not preferred because it generates additional thermal noise due to the resistors and also presents an added loading effect on the CG and CS outputs which affect the canceling accuracy. But on the other hand a disadvantage of CC stage is its additional distortion due to non-linear MOS-bipolar pseudo-resistor devices. Nevertheless this distortion will not be of major concern here as the signals will be chopped at the input of the CC stage as explained next.

In the block diagram shown for the front-end in Fig. 7, it can be seen that the chopping configuration is modified such that the dechopping of the NCCS outputs is now not performed at the CS outputs like mentioned in [14] but it is rather shifted to the output of the second stage. This is primarily done to ensure the dominant low frequency noise contributors in the CC stage namely $1/f$ noise of the OTA and the thermal noise of the pseudo-resistors also get upconverted in addition to $1/f$ noise of M_{cs} thereby avoiding any degradation in overall front-end noise performance. As a result of shifting dechopping to the output of the CC stage, chopping is now added to the CG stage outputs for proper operation.

In this chopping configuration, any distortion added in the CC stage can be easily filtered prior to dechopping by using a low-pass filter whose cutoff frequency is such that it is less than twice the chopping frequency.

C. Front-End

The circuit schematic of the entire two-stage fully differential biosensor front-end based on canceling and chopping techniques is shown in Fig. 8. The transimpedance $R_{m,fe}$ of the entire front-end is $R_{cg}C_{in}/C_{fb}$. Its overall distortion in the presence of canceling is determined by the CS, CC stages as the distortion of the CG stage gets canceled. Similarly its noise performance with noise canceling and chopping enabled is mainly limited by thermal noise and the overall I/P noise PSD under the matched condition is given by [7]

$$S_{n,fe}=\frac{8kT}{R_{cg}}\left(\gamma_{cgcs}+\frac{2}{R_{cg}}\left[\frac{1}{R_1(2\pi f_{chop}C_{in})^2}+\frac{\gamma\left(\frac{C_t}{C_{in}}\right)^2}{G_{m,ota}}\right]+\frac{.8525}{f_{chop}}\left[\frac{\gamma R_{cg}f_{k,cs}}{G_{m,cs}R_s^2}+\frac{2\gamma f_{k,ota}}{R_{cg}G_{m,ota}}\right]\right) \quad (18)$$

where $f_{k,ota}$ is the $1/f$ corner frequency of the the OTA input pair and C_t is the total capacitance including the parasitics at the OTA input node. The overall I/P noise as given by (18) is governed by the thermal noise contribution of the canceling stage (γ_{cgcs}) and apart from that it also includes other noise contributions namely the upconverted thermal noise of the pseudo-resistor after referring it to the input (second term), thermal noise of the OTA input pair (third term) and the residual $1/f$ noise of the CS stage, OTA as given by the last two terms respectively.

The common mode rejection ratio (CMRR) in this front-end is determined by the mismatches in the CG, CS and the CC stages. Among the different stage mismatches, the ones in the CS, CC stages do no greatly impact the CMRR as they will get upconverted due to chopping and only the mismatches in the CG stage are important. The resulting CMRR is then given by (derivation given in appendix C)

$$CMRR=\frac{R_{cg,p}-R_{cg,m}}{R_{cg,p}+R_{cg,m}}, \quad (19)$$

which as seen above is limited by mismatches in R_{cg} only while even the mismatches in M_{cg}, R_s do not greatly impact the CMRR for $k_{deg} \gg 1$.

In an actual biosensing application, the usefulness of the CMRR lies in rejecting the common-mode non-idealities of the

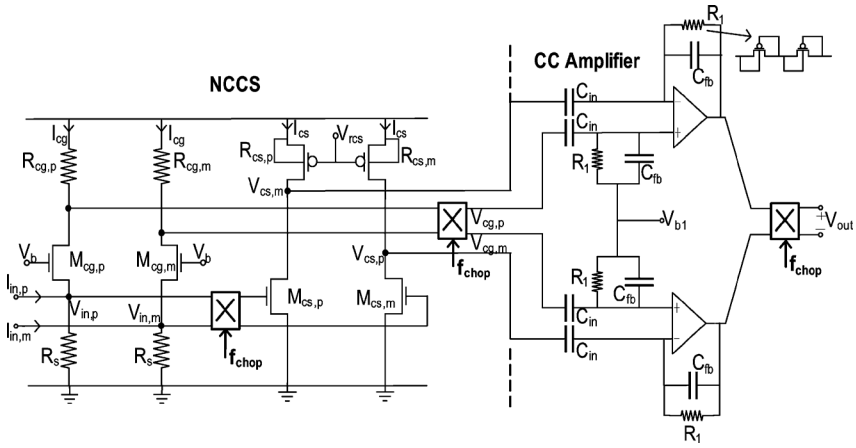

Fig. 8. Schematic of entire front-end.

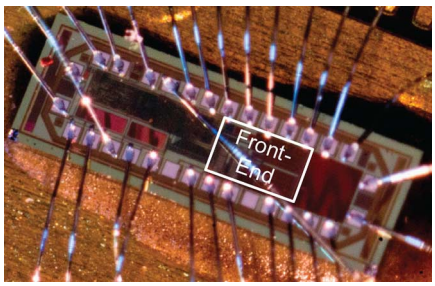

Fig. 9. Photograph of the integrated front-end.

biosensor which is achieved by detecting the reference (buffer) current in addition to the signal current [21].

VII. Circuit Design and Measurement Results

The presented front-end is validated in a 0.18 μm CMOS process and the die photo is shown in Fig. 9. The active circuit area is 350 μm$\times$ 500 μm.

In the NCCS amplifier, the CG stage is biased close to WI for low power consumption and the CS stage is biased close to SI ($V_{G,cs}-V_{T0} \approx 150\,\mathrm{mV}$) for low distortion. The bias current I_{cg} is chosen to have an input impedance R_{in} of nearly 2 kΩ which is less than the impedance of the microelectrodes (order of tens of kΩ or more). The bias current I_{cs} is chosen to be a fraction of I_{cg} sufficient enough to keep the thermal noise of the CS stage only a fraction of the CG stage thermal noise. Accordingly, I_{cs} is chosen nearly 3 times smaller than I_{cg} and this gives an excess thermal noise of nearly 30% for $V_{G,cs} - V_{T0} \approx 150\,\mathrm{mV}$ as seen from Fig. 3. R_{cg} is chosen as 60 kΩ to maximize the transimpedance in the NCCS stage. The linear region PMOS transistor which sets R_{cs} is sized to satisfy the canceling condition nominally. Sizing of M_{cs} is done so as to ensure its corner frequency $f_{k,cs}$ is less than the chopping frequency (chosen as 4 kHz) to minimize the residual white noise due to $1/f$ noise folding [7]. Sizing of M_{cg} need not be large enough to satisfy the condition $f_{k,cg} < f_{chop}$ as its $1/f$ noise is rejected by canceling. The bias voltages V_b and V_{rcs} in this chip are set externally instead of setting them using the biasing circuitry. This gives us experimental flexibility and also allows for a full characterization of the front-end.

In the CC gain stage, a single stage differential pair OTA with PMOS inputs is employed with its input transistors in WI to minimize its thermal noise and power consumption. Similar to the CS stage, the bias current of the CC stage is chosen to be a fraction of the CG stage sufficient enough to keep its thermal noise less than that of the CG stage. The CC amplifier is implemented as a variable gain stage with four different gain settings and the gain is varied through digital selection of the input capacitance C_{in}. The unit capacitance of C_{in} is chosen as 2.5 pF and this gives a fairly low cut-off frequency at the input of the CC stage. All the chopper switches used in the design are NMOS switches and they are sized minimally for decreasing the clock feedthrough and the charge injection effects. Different clock phases required for the choppers are generated on-chip from an external 4 kHz clock signal.

A. Front-End Characterization

Measurements were carried out using Agilent Spectrum Analyzer E4440A. Before feeding the CC amplifier outputs to the spectrum analyzer, an external buffer is used for differential to single ended conversion of the CC outputs. The noise floor of this external buffer measured independently is lower than the output noise of the front-end.

Transimpedance of the front-end is measured for four different gain settings in the CC amplifier and the achieved DC gains are given in Table I. Canceling property in the front-end is evaluated first by injecting a single tone voltage signal at the gate of one of the CG transistors (this is equivalent to the non-ideal currents generated in M_{cg}) and the control voltage V_{rcs} is varied. The front-end outputs are measured for two cases namely, with and without canceling. In the presence of canceling, the CS stage is active and hence based on the degree of matching of condition (8), the applied signal gets rejected. In the absence of canceling, the CS stage is disabled and only the CG stage along with the CC stage is active and there is no rejection for the applied signal. Fig. 10 shows a plot of the measured rejection as a function of V_{rcs} with the rejection being calculated as

$$\rho_1 = \frac{|V_{cc,1}|}{|V_{cc,2}|} \tag{20}$$

TABLE I
SUMMARY OF MEASURED FRONT-END PERFORMANCE

Supply Voltage		1.8 V
Total Current Consumption		50 μA
CG_{diff}		34 μA
CS_{diff}		10 μA
CC_{tot}		6 μA
DC Transimpedance Gain $R_{m,fe}$ (CC gain setting=2.5, 5, 7.5, 10)		150 KΩ, 292 KΩ, 426 KΩ, 550 KΩ
I/P Ref. Noise PSD		1.6 $pA/\sqrt{Hz}$
RMS I/P Noise Current (100 Hz BW)	Canceling, Chopping	22 pA
	CG Only	62 pA
	w/o Canceling, Chopping	132 pA
THD @ 1 uA Input, Min Gain	Canceling	-55 dB
	No Canceling	-38 dB

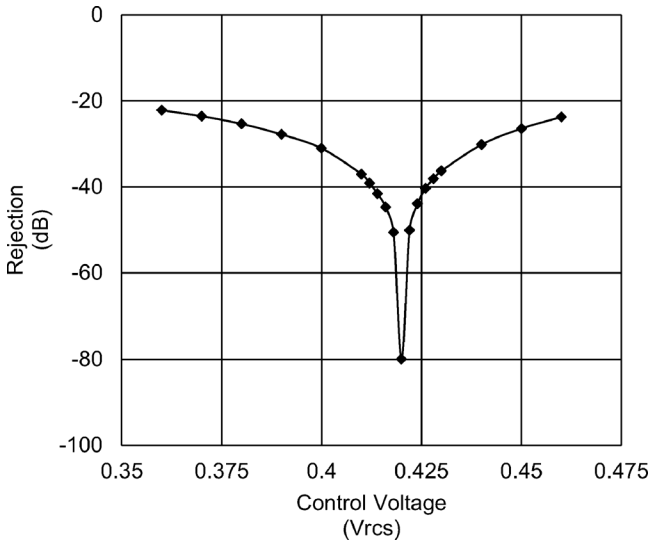

Fig. 10. Measured rejection as a function of the control voltage V_{rcs} for a single tone (28 Hz) voltage signal injected at the gate terminal of the CG stage to evaluate the canceling property in the front-end.

where $V_{cc,1}$, $V_{cc,2}$ are the respective CC amplifier outputs with and without canceling. From the plot shown in Fig. 10, maximum rejection achieved is nearly -80 dB for which the canceling condition is satisfied with a greater accuracy. On either side of this point, rejection degrades which is due to inaccurate canceling owing to deviation from the canceling condition.

In Fig. 11, the spectral rejection plot at a constant V_{rcs} is shown. With canceling being active, rejection of the fundamental and the third harmonic is clearly evident. In the case of the second harmonic however, the magnitude is higher than for the case of without canceling which is due to the fact that the CS or the CC stage dominates the second harmonic after cancelation.

Fig. 12 shows the plot of the measured input referred noise density in the overall front-end with and without $1/f$ noise rejection techniques. As evident from the noise plot, the effect of $1/f$ noise is minimized in the presence of canceling and chopping. Also the low frequency noise floor is dominated mostly by thermal noise except for the residual $1/f$ noise which is due to mismatches in the cancelation condition and the limited

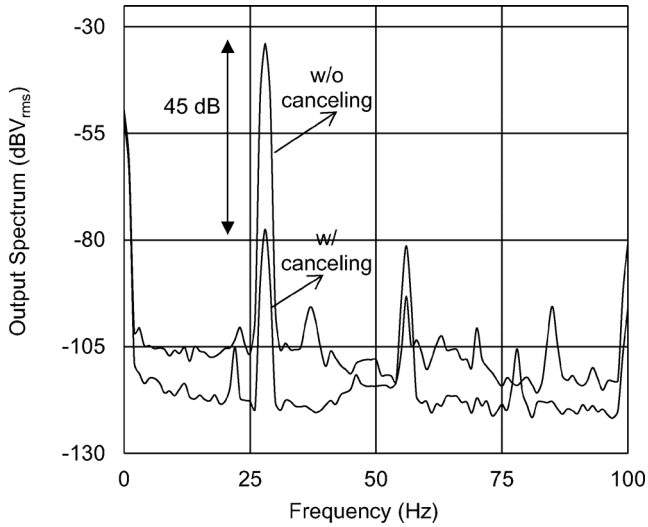

Fig. 11. Output spectrum showing the rejection for a single tone (28 Hz) voltage signal injected at the gate terminal of the CG stage in the presence of canceling.

canceling accuracy. This residual $1/f$ noise is however not a major concern as anyway the input referred RMS noise current with canceling, chopping active is lower by at least three times in comparison to the other two cases as seen from the corresponding values given in Table I.

In the inset of the noise plot, the thermal noise floor for the three different cases are shown for higher frequencies alone. The slight increase in thermal noise with canceling and chopping active can be seen which is attributed to the excess thermal noise contribution of the CS and CC stages. Also evident in the plot for the case of canceling, chopping is the upconverted noise of all the low frequency dominant noise sources in the front-end. The noise floor for the case of without canceling, chopping is seen decreasing in the plot because of the filtering effect caused by the output parasitics.

The input referred current noise density in the overall front-end with canceling and chopping active is measured to be 1.6 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ which closely matches with the simulated/expected value of 1.8 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

Next distortion in the front-end is characterized with and without canceling for a single tone input current I_{in} of 1 μA and with the gain being set to minimum in the CC stage. The plot in Fig. 13 shows the normalized output spectrum where the property of distortion canceling is evident as seen from the attenuation of both the 2^{nd} and the 3^{rd} harmonic distortion components when canceling is active. The observed distortion levels subsequent to the cancelation of the CG distortion correspond to the effective distortion of the CS, CC stages. Further it can also be noticed that due to distortion canceling, only the harmonic distortion components are attenuated whereas the fundamental component is not attenuated which is because the CS stage cancels only the distortion of M_{cg} but not the input signal itself and instead amplifies the input signal by a small factor.

Shown in Fig. 14 is the corresponding plot of THD as a function of V_{rcs} for a peak input current of 1 μA. In the absence of canceling, THD remains constant at -38 dB because only

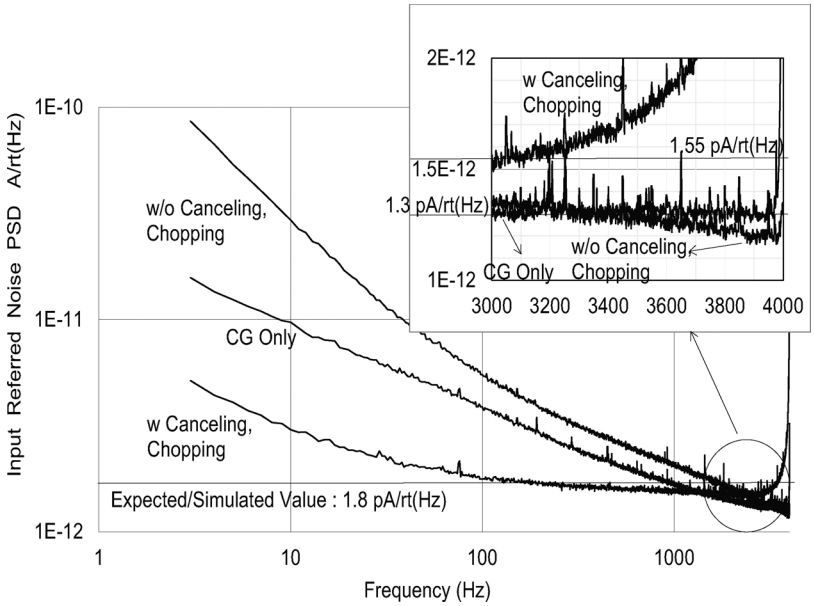

Fig. 12. Measured input referred noise density with and without $1/f$ noise rejection techniques. (Values below 3 Hz could not be shown because of spectrum analyzer limitations.)

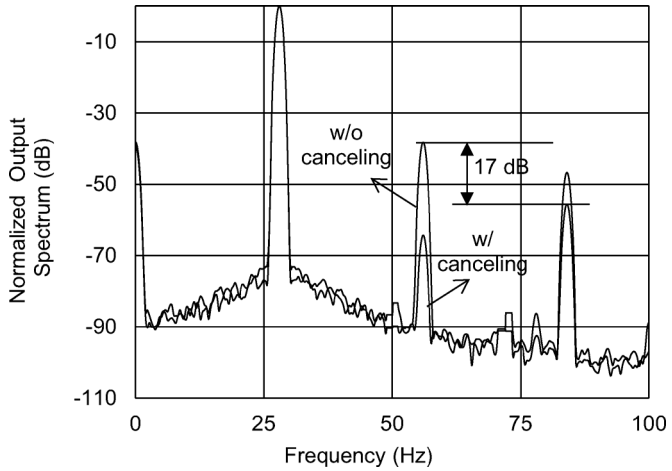

Fig. 13. Normalized output spectrum showing the distortion canceling property for a single tone (28 Hz) peak input current I_{in} of 1 μA.

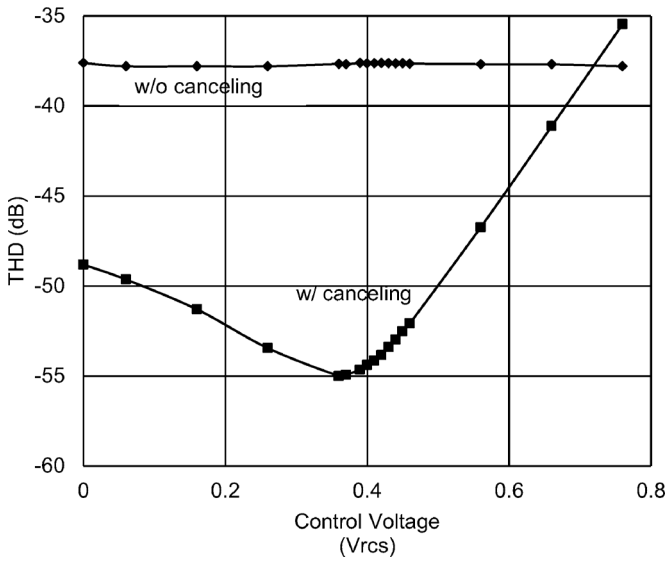

Fig. 14. THD as a function of the control voltage V_{rcs} for a peak input current I_{in} of 1 μA.

the CG stage along with the CC amplifier is active and there is no distortion canceling. On the other hand, THD with distortion canceling (or with the CS stage active) varies with V_{rcs} and achieves a minimum. On either side of the minimum, THD begins to increase because of the degrading canceling condition. The minimum THD achieved is nearly -55 dB which is 17 dB lower in comparison to without canceling. Further it can also be noticed from this plot that even while the variations in V_{rcs} are large that are similar to process, temperature variations etc., the achieved THD in the presence of canceling is still only lower which shows the robustness of the canceling technique and moreover it also remains lower for as long as the variations do not get large enough to push R_{cs} into saturation from linear region (In this case, this happens only for variations greater than 200 mV or so on the high side of the optimum point as seen from the plot).

The overall performance measured in the front-end is also summarized and given in Table I under different conditions.

B. Electrochemical Measurements

The presented front-end has been tested with electrochemical sensors and as part of a wireless sensing system which is a prototype for the target application. The prototype system includes microfabricated electrochemical sensors for the characterization of biomolecular layers and a full system-on-chip (SoC) in addition to the front-end. The details related to the microelectrodes fabrication and the CV measurements conducted with the front-end are given below while the details of the SoC can be obtained from [23].

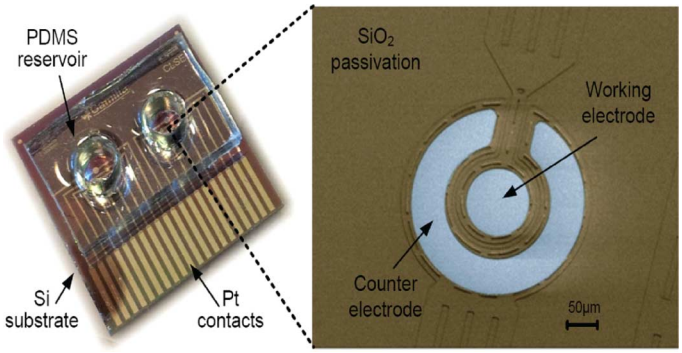

Fig. 15. Camera photo of the fabricated chip (left) and the SEM photo of the WE and CE with the SiO_2 passivation.

1) Microelectrode Fabrication: Platinum working electrode (WE) and counter electrode (CE) are fabricated on a 100 mm diameter silicon wafer with 1 μm thick thermally grown oxide passivation layer. First, a standard double-layer lift-off process is used to pattern the electrodes. Then, the wafer surface is covered by SiO_2 sputtering to passivate the interconnections. Finally, the passivation layer on the electrodes and the socket contacts are etched by reactive-ion-etching (RIE) by using the patterned photoresist as the masking layer. More details on the fabrication process is given in [24]. After dicing the chips, the surface is cleaned with Acetone, IPA, and O_2 plasma, respectively. Finally, a PDMS chamber is used as the reservoir for the solutions during the CV measurements. Fig. 15 shows the camera photo of the chip after PDMS reservoir placement, and the SEM micrograph of the microelectrode.

2) Cyclic Voltammetry (CV) Test Results: After an Ar plasma treatment to remove the native oxide layer on the Pt electrode surface, the chip is incubated overnight in 1 mM ethanolic solution of 6-(Ferrocenyl)hexanethiol. Thus, a self-assembled monolayer (SAM) is obtained with ferrocene functionalized alkanethiols. Ferrocene, which is an electrochemical label, can be employed as a covalent label for electrochemical aptamer based sensors (aptasensors), such as for DNA or RNA detection. In this work, the possibility to detect the ferrocene on the surface is investigated by measuring the current generated in response to the redox activity. The chip is plugged to a PCB board through a card-edge socket, which allows to address 10 WEs and 10 CEs independently. The triangular wave having 100 mV/s scan rate is generated by LabView software. This signal is applied to the solution through the CE and an external Ag/AgCl reference electrode (RE) connected to a generic potentiostat circuit, which is implemented by external components for experimental flexibility. The generated current is measured by the front-end as the electrodes are in 0.1 M $HClO_4$, 10 mM HCl solution. Fig. 16 shows the CV result of the 100 μm diameter WE as detected by the front-end for a CV input swept from -0.1 V to 0.4 V.

VIII. Performance Comparison

The front-end performance achieved in this work is compared with the other works in terms of current consumption, linear range over a certain bandwidth, linearity and a summary is given in Table II. From the table, firstly comparing the front-end (shown in bold) to the case of without canceling and chopping, the improvement achieved in both sensitivity and linearity are evident thanks to the use of canceling and chopping. Moreover it can also be noticed that this improvement has been achieved at the expense of only fractionally higher current. Next in comparison to the chopped CG TIA, it can be seen that the latter achieves a marginally better sensitivity and also consumes slightly lesser as there is no CS stage and also one CC amplifier is sufficient for the second gain stage. But then the disadvantage as seen from the table is its higher distortion which is five times more.

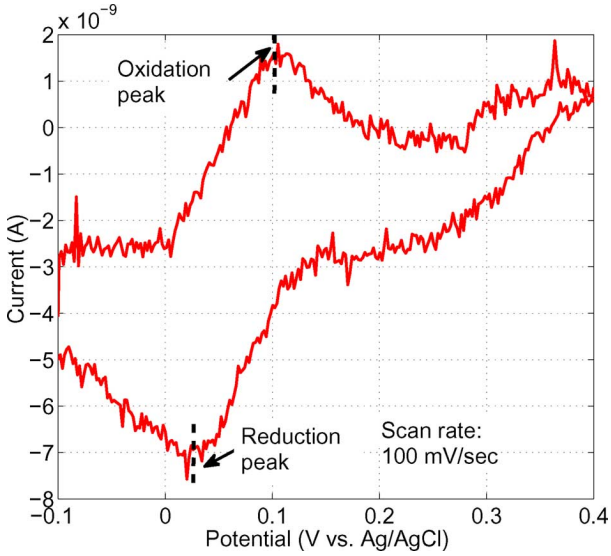

Fig. 16. CV of the 100 μm diameter electrode after incubation with 6-(Mercaptohexyl) ferrocene. (The current value is extracted by dividing the voltage output of the front-end by the transimpedance gain.)

A figure-of-merit (FOM) [25] is also used to evaluate overall performance in the front-end which is given by

$$FOM = \sqrt{\frac{P}{kT \cdot BW}} \frac{K}{DR} \tag{21}$$

with P being the power consumption in Watts, BW being the bandwidth in Hz, DR being the dynamic range (expressed as a ratio and not in dB) and K being the linearity in %. According to this FOM, a front-end with an overall better performance achieves the least FOM value. Note that although an FOM like NEF [26] already exists for sensor front-ends, it is not preferred here because of the fact that in current mode front-ends there exists a current-distortion trade-off due to which the minimum current consumption atleast in the first gain stage is set by linearity too apart from noise. Hence using an FOM like NEF wont be appropriate here as it takes into account only thermal noise whereas the above given FOM includes linearity in addition to noise and current consumption thereby giving a more fair comparison of different works.

Comparing different conditions in the front-end based on the FOM, it can be seen that the FOM values achieved with canceling and chopping are smaller relative to the other two cases by one and two orders of magnitude. Particularly, the FOM achieved relative to the chopped CG TIA is lower by nearly four

TABLE II
SUMMARY OF PERFORMANCE COMPARISON

Ref.	Supply (V)	Current Consumption	BW (Hz)	Linear Range	Linearity (%)	FOM	Comment
Reay et al [8]	4.8	1 mA	330	100 fA-819 pA 4.8 nA-40 uA	.0122 .0122	44	AZ,[1] Opamp based Integrator FE
Roham et al [22]	2.5	29 uA	5K	56 pA-750 nA	.005	.349	Opamp based Integrator FE
Levine et al [9]	2.5	$>$ 4 mA	2500	240 pA-110 nA	.2	$>$ 6780	AZ, Opamp based Integrator FE
Genov et al [6]	9	1.38 mA	12K	46 pA-50 uA	1	7	No CS,[2] No AZ, CG TIA based FE with reconfigurable gain
Narula et al [5]	2.5	52 uA	.4	1 pA-200 nA	.1	70	No CS, No AZ, CG TIA based FE
Manickam et al [3]	3.3	150 uA	10	330 pA-40 uA	10	4510	No CS, No AZ, CG TIA based FE
Turner et al [4]	5	400 uA	–	100 nA-3.5 uA	2	–	No CS, No AZ, CG TIA based FE
This Work	**1.8**	**50 uA**	**100**	**22 pA-1 uA**	**.2**	**29**	**With Canceling, CS**
	1.8	37 uA	100	17 pA-1 uA	1	110	Chopped CG TIA
	1.8	40 uA	100	132 pA-1 uA	1	888	No Canceling, No CS

[1] Autozeroing
[2] Chopper Stabilization

times even while the current consumption and the noise level are slightly higher which justifies the motivation for choosing the canceling based front-end in this work.

Similarly comparing the present work with other front-ends using the FOM, it can be seen that the performance achieved in this work is better than [3]–[5], [8], [9] and also competitive in comparison to [6], [22]. Nevertheless in comparison to [8], [22], the linearity achieved in this work is not better which is because the front-end presented here is based on open loop distortion minimization techniques whereas a closed loop opamp based front-end has been employed in [8], [22].

IX. CONCLUSION

A novel low power front-end for current-mode biosensors with low noise, low distortion features has been presented. The crucial circuit blocks that are responsible for low power-low distortion and low noise in the front-end are the noise canceling TIA and the NCCS amplifier respectively. In the noise canceling TIA, we have made best use of the advantages of WI and SI in the presence of distortion canceling to achieve low power and low distortion simultaneously. The distortion levels achieved thereby are lower relative to a CG TIA by a significant factor. In the NCCS amplifier, we have taken advantage of the canceling property inherent to the noise canceling TIA and combined it with chopping to reject $1/f$ noise completely. Relative to a chopper stabilized CG TIA, the NCCS amplifier achieves lower distortion for only a slightly higher noise floor. While we achieve low noise and low distortion by using the above techniques, we do not compromise at the same time in terms of either the excess current or the excess thermal noise which are only fractionally higher.

The presented front-end is validated in a 0.18 μm CMOS process and it consumes only 50 μA from a 1.8 V supply voltage. The measured input referred noise density is $1.6\,\mathrm{pA}/\sqrt{(\mathrm{Hz})}$ and the THD achieved for a peak current of 1 μA is -55 dB.

Comparison of the achieved performance with other existing works shows that the canceling based front-end presented in this work is both competitive and better than most other open loop biosensor front-ends and this is justified from the FOM given in Table II.

APPENDIX A
DISTORTION COEFFICIENTS FOR THE CG STAGE

Assuming the CG transistor is in WI, the current flowing through M_{cg} is given by

$$I_t = I_{cg} - \Delta I_{cg} = I_{spec} \cdot \exp\left[\frac{V_b - V_{T0}}{nU_T} \cdot \frac{-(V_{in} + \Delta V_{in})}{U_T}\right] \tag{22}$$

where $I_{spec} = 2n\beta_n U_T^2$ is the specific current, I_{cg} is the quiescent current and ΔI_{cg} is the current due to the voltage variations ΔV_{in} at the source node of M_{cg} in the presence of input current I_{in}. The dependance of the current ΔI_{cg} on ΔV_{in} is non-linear and hence (22) can be written in its taylor series form as

$$I_{cg} - \Delta I_{cg} \approx I_{cg}\left[1 - \frac{\Delta V_{in}}{U_T} + \frac{\Delta V_{in}^2}{2U_T^2} + \cdots\right]$$
$$\Delta I_{cg} = I_{cg}\left[\frac{\Delta V_{in}}{U_T} - \frac{\Delta V_{in}^2}{2U_T^2} + \cdots\right]. \tag{23}$$

In (23), only the second order term is dominant while the higher order terms can be neglected (verified from simulations). Using the relation $\Delta I_{cg} = I_{in} - \Delta V_{in}/R_s$ and applying it in (23), ΔV_{in} and ΔI_{cg} can be simplified and it can be shown that

$$\Delta V_{in} \approx R_{in} I_{in} + \frac{U_T}{2I_{cg}^2} I_{in}^2$$

$$\Delta I_{cg} = \alpha_1 I_{in} - \alpha_2 I_{in}^2 = I_{l,cg} + I_{nl,cg}. \tag{24}$$

Equation (24) is the non-linear current equation for a CG stage in WI where $\alpha_1 = k_{deg}/(k_{deg}+1) \approx 1$ and $\alpha_2 = 1/(2I_{cg}k_{deg})$.

Appendix B
Distortion Coefficients for the CG-CS Stage

The output voltage of the canceling stage ignoring the noise contributions is given by

$$\Delta V_{cgcs} = I_{in}R_{cg} + I_{nl,cs}R_{cs} = \left(I_{in} + \frac{I_{nl,cs}}{G_{m,cs}R_s}\right) R_{cg}. \tag{25}$$

For M_{cs} in SI, the distortion current $I_{nl,cs}$ can be derived using the ideal MOS equation and it can be easily shown that $I_{nl,cs} \approx (\beta_{cs}/2n)\Delta V_{in}^2 = (\beta_{cs}/2n)I_{in}^2 R_{in}^2$ [18] with $\beta_{cs} = (\mu_n C_{ox})(W/L)_{cs}$, n being the slope factor. Knowing $I_{nl,cs}$, the non-linear CGCS output can be reduced to

$$\Delta V_{cgcs} = \left(I_{in} + \frac{\beta_{cs}}{2n}\frac{R_{in}^2}{G_{m,cs}R_s} I_{in}^2\right) R_{cg} = \left(\theta_1 I_{in} + \theta_2 I_{in}^2\right) R_{cg} \tag{26}$$

where $\theta_1 = 1$ and $\theta_2 = (\beta_{cs}/2n)(R_{in}^2/[G_{m,cs}R_s]) = U_T/(2I_{cg}[V_{g,cs} - V_{T0}]k_{deg})$ with U_T being the thermal voltage.

Appendix C
CMRR of the Front-End

The CMRR of the front-end is defined here as

$$CMRR = \frac{R_{m,fe,c}}{R_{m,fe,d}} \tag{27}$$

where $R_{m,fe,d} = \Delta V_{fe,d}/I_{in}$ and $R_{m,fe,c} = \Delta V_{fe,c}/I_{in}$ are the differential mode (DM) and the common mode (CM) front-end gains respectively and $\Delta V_{fe,d}$, $\Delta V_{fe,c}$ are the respective DM and CM front-end outputs.

For differential mode operation ($I_{in,p} = -I_{in,m} = I_{in}/2$), $\Delta V_{fe,d}$ is given by

$$\Delta V_{fe,d} = (\Delta V_{cg,d} - \Delta V_{cs,d})\frac{C_{in}}{C_{fb}} \tag{28}$$

with $\Delta V_{cg,d}$, $\Delta V_{cs,d}$ being the respective differential outputs.

From Fig. 6, $\Delta V_{cg,d}$ is given by

$$\Delta V_{cg,d} = \frac{I_{in}R_{cg}}{2}\left(\frac{1+\delta_1}{1+\frac{1}{k_{deg}(1+\delta_k)}} + \frac{1-\delta_1}{1+\frac{1}{k_{deg}(1-\delta_k)}}\right) \tag{29}$$

where δ_1 is the mismatch coefficient in R_{cg}, δ_k is the mismatch coefficient in k_{deg} which includes the mismatches of R_s as well as $G_{ms,cg}$. Using the approximation $1/(1+1/(k_{deg}[1\pm\delta_k])) = 1 - 1/(k_{deg}[1\pm\delta_k])$ $\Delta V_{cg,d}$ can be rewritten as

$$\begin{aligned}\Delta V_{cg,d} &= \frac{I_{in}R_{cg}}{2}\left(\frac{1+\delta_1}{\left(1-\frac{1}{k_{deg}(1+\delta_k)}\right)^{-1}} + \frac{1-\delta_1}{\left(1-\frac{1}{k_{deg}(1-\delta_k)}\right)^{-1}}\right) \\ &= \frac{I_{in}R_{cg}}{k_{deg}}\left([k_{deg}-1] + \delta_1\delta_k\right).\end{aligned} \tag{30}$$

In (30), the factor $\delta_1\delta_k$ is the contribution of mismatches in k_{deg} and this creates an additional mismatch current that flows through R_{cg} resistors. But their contribution is only negligible as $k_{deg} - 1 \gg \delta_1\delta_k$ and hence

$$\Delta V_{cg,d} = \frac{I_{in}R_{cg}}{k_{deg}}\left(k_{deg} - 1\right). \tag{31}$$

The differential CS output $\Delta V_{cs,d}$ can also be derived from Fig. 6 for $k_{deg} \gg 1$ and is given by

$$\begin{aligned}\Delta V_{cs,d} &= \frac{I_{in}}{2G_{ms,cg}}\frac{R_{cg}}{R_s}\left(\frac{1}{1+\delta_{gms}} + \frac{1}{1-\delta_{gms}}\right) \\ &= \frac{I_{in}R_{cg}}{k_{deg}}\end{aligned} \tag{32}$$

where δ_{gms} is the mismatch coefficient of $G_{ms,cg}$. In (32), we have assumed the canceling condition is satisfied ($R_{cg}/R_s = G_{m,cs}R_{cs}$) and chopping is enabled. With chopping enabled, mismatches in the CS stage do not have an influence as their mismatch contributions get upconverted.

For common mode operation ($I_{in,p} = I_{in,m} = I_{in}/2$), the CM mode outputs $\Delta V_{cg,c}$, $\Delta V_{cs,c}$ can also be derived from Fig. 6 which are given below for $k_{deg} \gg 1$.

$$\begin{aligned}\Delta V_{cg,c} &= \frac{I_{in}R_{cg}}{2}\left(\frac{1+\delta_1}{1+\frac{1}{k_{deg}(1+\delta_k)}} - \frac{1-\delta_1}{1+\frac{1}{k_{deg}(1-\delta_k)}}\right) \\ &= \frac{I_{in}R_{cg}}{k_{deg}}\left(\delta_1[k_{deg}-1] + \delta_k\right) \\ &\approx \frac{I_{in}R_{cg}\delta_1(k_{deg}-1)}{k_{deg}}\end{aligned} \tag{33}$$

$$\begin{aligned}\Delta V_{cs,c} &= \frac{I_{in}}{2G_{ms,cg}}\frac{R_{cg}}{R_s}\left(\frac{1}{1+\delta_{gms}} - \frac{1}{1-\delta_{gms}}\right) \\ &= \frac{I_{in}R_{cg}}{k_{deg}}\delta_{gms}\end{aligned} \tag{34}$$

Using (31) and (32) the differential mode gain $R_{m,fe,d}$ is

$$R_{m,fe,d} = (\Delta V_{cg,d} - \Delta V_{cs,d})\frac{C_{in}}{C_{fb}} = R_{cg}\frac{C_{in}}{C_{fb}}. \tag{35}$$

Using (33) and (34) the common mode gain $R_{m,fe,c}$ is

$$R_{m,fe,c} = (\Delta V_{cg,c} - \Delta V_{cs,c})\frac{C_{in}}{C_{fb}} = \delta_1 R_{cg}\frac{C_{in}}{C_{fb}}. \qquad (36)$$

Accordingly the common mode rejection as defined by (27) is

$$CMRR = \frac{R_{m,fe,c}}{R_{m,fe,d}} = \delta_1 = \frac{R_{cg,p} - R_{cg,m}}{R_{cg,p} + R_{cg,m}} \qquad (37)$$

which shows that the common mode rejection is limited only by the mismatches in R_{cg}. This is because mismatches in k_{deg} are negligible for $k_{deg} \gg 1$ and mismatches in CS, CC stages do not influence the CMRR thanks to chopping.

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