A 16 × 16 CMOS Capacitive Biosensor Array Towards Detection of Single Bacterial Cell

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***Abstract*—We present a 16 × 16 CMOS biosensor array aiming at impedance detection of whole-cell bacteria. Each 14 μm × 16 μm pixel comprises high-sensitive passivated microelectrodes connected to an innovative readout interface based on charge sharing principle for capacitance-to-voltage conversion and subthreshold gain stage to boost the sensitivity. Fabricated in a 0.25 μm CMOS process, the capacitive array was experimentally shown to perform accurate dielectric measurements of the electrolyte up to electrical conductivities of 0.05 S/m, with maximal sensitivity of 55 mV/fF and signal-to-noise ratio (SNR) of 37 dB. As biosensing proof of concept, real-time detection of *Staphylococcus epidermidis* binding events was experimentally demonstrated and provides detection limit of ca. 7 bacteria per pixel and sensitivity of 2.18 mV per bacterial cell. Models and simulations show good matching with experimental results and provide a comprehensive analysis of the sensor and circuit system. Advantages, challenges and limits of the proposed capacitive biosensor array are finally described with regards to literature. With its small area and low power consumption, the present capacitive array is particularly suitable for portable point-of-care (PoC) diagnosis tools and lab-on-chip (LoC) systems.**

***Index Terms*—Bacteria detection, correlated double sampling (CDS), impedance sensor, multi-electrode array (MEA), real-time.**

I. Introduction

INTEGRATED biosensor arrays can combine thousands biosensor units on a single chip, making them unique platforms for multiplex diagnosis. Many studies have highlighted the huge medical potential of charged-based multi-electrode arrays (MEA) to sequence bacterial and human genome in few hours [1] and record real-time activities of electrogenic cells from the brain and heart [2], [3].

Such array can also be envisioned for point-of-care (PoC) detection of pathogen bacteria, where the huge amount of parallel detectors can provide multiplexing and reduce the sample size, diagnosis time, cumbersomeness and cost [4]. Another key advantage is that pixels can be shrunk to the micrometer size while keeping the same total sensing area by increasing their number. As close to the bacterial size ($\sim \mu$m), each sensor unit increases its sensitivity and can then envision detection of single whole-cell bacterium. This is highly desirable since the whole biosensor array thus strongly enhances its detection limit in term of number of bacteria per mm^2 [5], and can serve as substitute to concentration techniques such as dielectrophoresis [6]or magnetic beads [7].

For whole-cell bacterial sensing, impedance spectroscopy and capacitive sensing are typically preferred to charge sensing because of the huge spectral information and the excellent sensitivity and specificity [8]. Using nanometer Al_2O_3 passivation [9], recent works have demonstrated the use of CMOS-compatible interdigitated microelectrodes (IDE) of 300 μm length and 4 μm gap as capacitive biosensors to selectively detect whole-cell *Staphylococcus epidermidis* in various solutions [10], [11]. However, these studies report a minimum detectable number of ca. 10^3 bacteria per mm^2, which intrinsically restrains the limit of detection (LoD) in the range of 10^7 CFU/mL after 10 minutes of incubation. Biosensor arrays with various capacitive interfaces have been reported for detection of cells [12], DNA [13]–[16], proteins [17] or 10 μm polystyrene or magnetic beads [12], [18], but not for whole-cell bacteria to the best knowledge of the authors. In the case of nanometer biospecies such as proteins and DNA, the sensing units monitor an interfacial capacitive change in the electrical double layer (DL), uniformly affected by biospecies. In contrast, cells and beads that are larger than 10 μm typically exceed the pixel size, so that sensors evaluate their volumic dielectric properties. For bacterial cells, the same principle can be used but the modified volume between electrodes is three orders of magnitude smaller because of their 1 μm diameter. In this case, sensitivity is then the key performance to enhance.

In this paper, we report the first CMOS capacitive biosensor array for detection of whole-cell bacteria. Built in a 0.25 μm mixed-signal CMOS process, the 16 × 16 array comprises pixels of 14 μm × 16 μm whose sensing parts include two Al_2O_3-passivated microelectrodes in the last CMOS metal layer. The in-pixel readout circuit uses a non-differential charge sharing principle combined with a gain transistor in subthreshold operation to enhance the sensitivity to bacterial cells. The working principle is experimentally assessed in various solutions of different permittivity and real-time detection of *Staphylococcus epidermis* is eventually demonstrated.

The paper is organized as follows. In Section II, the challenges of capacitance conversion inside micrometer-sized pixels towards biosensing are addressed. In Section III, the designs of the electrical circuit and sensing parts are detailed. In Section IV, experimental performances achieved by the capacitive array are described in dry condition and in solutions

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with and without bacterial cells. Finally, a comparison with capacitive biosensor arrays from the literature is provided in Section V.

II. Challenges of In-Pixel Capacitance Conversion

Capacitive readout interfaces convert in-pixel capacitances into either analog voltages, which then require analog-to-digital converters (ADC), or square voltages with capacitance-dependent frequency. As the circuit is integrated inside each pixel, the main challenge arises from the small pixel area required to boost sensitivity to bacteria. Several issues must then be considered to choose and design the readout interface:

- Sensed capacitances are typically extremely small ($\sim$ 10 fF) despite the large value of the solution permittivity. Parasitic capacitances and kT/C noise can thus possibly deteriorate sensing performance.
- Sensing electrodes patterned in the last CMOS metal layer are typically protected by a thin insulator layer [11], which partially screens the capacitances to sense.
- Biological solutions are typically high-conductive. The low resistance in parallel with the sensed capacitance can then trouble the capacitance conversion.
- Local mismatch between small pixels must be reduced, to enhance the fixed-pattern noise (FPN).

Among existing architectures, the differential method consists in subtracting the sensor capacitance to a reference capacitance [13], [14], [19], [20]. Despite its very high sensitivity, this technique is not appropriate for biosensor arrays. Indeed, each pixel must contain two sets of electrodes corresponding to sensed and reference capacitances, respectively. The last must provide a control value in the biological point of view, i.e., must be free of bacterial cells. This can be achieved either with an antifouling electrode coating that prevents bacterial cells to bind on the electrode surface or by locally flowing the same solution but without bacterial cells. Both approaches are currently not technically feasible as pixels are scaled down to the micrometer size and the last further requires the possibility to obtain the reference solution from the initial biological sample. Pseudo-differential methods also exist and consists in subtracting the sensed capacitance from an on-chip fixed capacitance [12]. In this case, versatility is the main issue since the fixed capacitance is calibrated for a given liquid with fixed permittivity and electrical conductivity.

Among single-ended methods, the charge-based method has the disadvantage to give output voltages inversely proportional to sensed capacitances [11], [17], [18]. Furthermore, charging time constants can become extremely small at high electrolyte conductivity [21]. Capacitor dividers are also not recommended as one electrode side is floating and then presents trap charges that strongly increases FPN. Coherent detection dealing with sinusoidal signal requires complex electrical circuitry and can hardly be integrated within a micrometer-sized pixel [15]. Finally, in-pixel capacitance-to-frequency conversion such using oscillators [11] suffer from high FPN as miniaturized, since no compensation technique exists.

Charge sharing principle [22] or switched capacitors [12] are thus the most appropriate techniques for targeted applications because of the implementable FPN compensation scheme and the linear high-sensitive dependence between the output voltage and the input capacitance. Depending on the switching frequency, they can be used in high-conductive electrolytes.

III. Implementation

In this section, the design of the biosensor array is fully detailed. The general architecture is first reviewed in Section III-A. Then, the design of sensing parts and electrical circuits within pixels are described in Sections III-B and III-C. Finally, the column amplifier design is investigated in Section III-D.

A. System Architecture

The biosensor array is divided in five parts: the row decoder, column decoder, pixel array, column amplifiers and output stage. The analog-to-digital conversion is not performed on-chip but with an off-chip instrument (cfr Section IV-A). The 4:16 decoders use two 2:4 decoders built with inverters and NAND gates. Other blocks are implemented as depicted in Fig. 1. The readout is controlled by digital signals synchronized on a 40 MHz clock and is composed of four main phases: the initialization, reset, integration and readout phases. The supply voltage V_{dd} is fixed to 2.5 V.

Each pixel comprises both sensing and readout parts. The sensor is implemented by miniaturized interdigitated microelectrodes (IDE) patterned in the last CMOS metal layer, covered with a thin post-processed passivation layer which is in contact with the solution under test. The underlying electrical circuit uses charge sharing principle to convert the IDE capacitance C_{IDE} into a proportional output voltage. One row of the capacitive array is read at a time and controlled by row decoders. The critical in-pixel nodes V_{IDE} and V_{gT} are first initialized to ground during the initialization phase. In reset phase, the transistor M_R set the voltage V_{pix} to its reset value and switches M_{C1} and M_{C2} load the voltage V_{gT} to a value proportional to the IDE capacitance

$$V_{gT} = \left(\underbrace{\frac{C_{IDE}}{C_{IDE} + C_D + C_{gT}}}_{\beta} \right) \cdot V_{ref} \simeq \left(\frac{C_{IDE}}{C_D + C_{gT}} \right) \cdot V_{ref} \quad (1)$$

with C_{gT} the gate capacitance of M_T, C_D the in-pixel capacitance of fixed value and V_{ref} the reference voltage supplied off-chip and applied to all pixels. This conversion comes from the charge redistribution between C_{IDE}, first loaded to V_{ref} as M_{c1} is asserted by V_{c1}, and the fixed capacitance $C_D + C_{gT}$ as M_{c2} is enabled by V_{c2}. By placing M_T in subthreshold inversion, the small value of V_{ref} enables maximizing the relative sensitivity S_r, defined as

$$S_r \triangleq \frac{1}{V_{out}} \cdot \frac{\partial V_{out}}{\partial C_{sol}} \quad (2)$$

where C_{sol} is the medium capacitance that can be slightly different from C_{IDE} (see Section III-B for more details) and

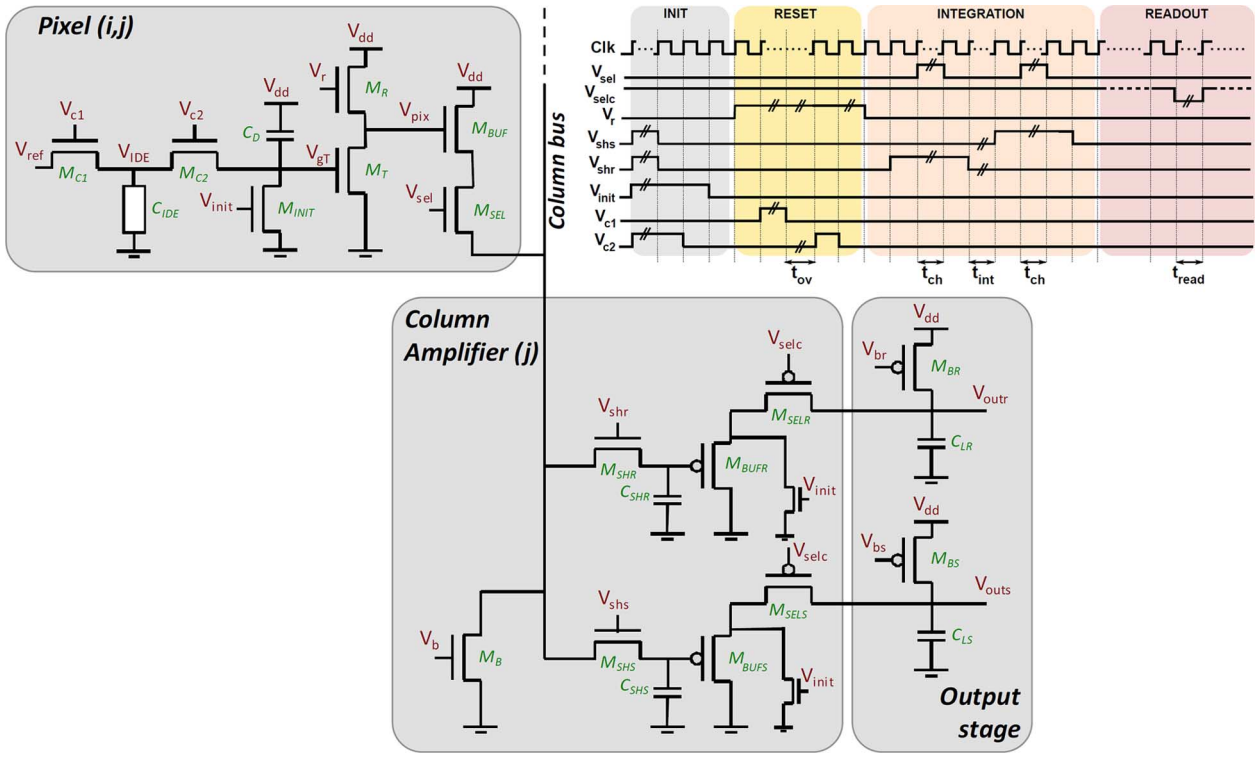

Fig. 1. System architecture of the pixel, column amplifier and output stage. The temporal diagram illustrates the digital controls for the readout of a single row, where annotations // refer to durations longer than the clock period. Four main phases are highlighted: the initialization, reset, integration and readout phases. The clock frequency is 40 MHz and the supply voltage V_{dd} is 2.5 V.

$V_{out}$the output voltage defined by (3). To maximize S_r, the voltage V_{gT} is amplified by an exponential transfer function (see Appendix A), provided by the subthreshold operation of M_T. SPICE simulations give a subthreshold slope of 98 mV/dec for M_T, corresponding to $\alpha = 98\,\text{mV}/\ln 10 = 42\,\text{mV}$ in Appendix A. Therefore, the subthreshold transfer function enhances the relative sensitivity S_r as $V_{gT} > 42$ mV.

During the integration phase, V_{gT} remains fixed to the value given by (1) since M_{c1} and M_{c2} are both disabled. The drain current of M_T progressively discharges V_{pix} during an integration period t_{int}, reducing its temporal noise. Both reset and signal values on V_{pix}, chosen at the start and end of integration period, are stored on column-based amplifiers. Eventually, for each in-row pixels selected by the column decoder, the readout phase successively sends reset and signal values stored in column amplifiers to the output stage, with corresponding voltages V_{outr} and V_{outs}, respectively. These analog signals are then converted to digital values by off-chip ADC, and the subtraction of signal from reset digital values implements the correlated double sampling (CDS) that reduces FPN and kT/C noise [23]

$$\begin{aligned} V_{out} &\triangleq V_{outr} - V_{outs} \\ &\propto \exp(V_{gT}) \\ &\propto \exp(C_{IDE}) \end{aligned} \tag{3}$$

where the two last relationships hold as M_T is in subthreshold inversion. The major contributions with regards to the charge sharing implementation proposed in [22] are the additional subthreshold gain stage, the calibration capability with V_{ref} and the large on-chip capacitance C_D, providing a better linear relationship between V_{gT} and C_{IDE}.

B. Design of the Pixel Sensing Part

For each pixel, two electrodes are patterned in the last CMOS metal layer and connected to V_{IDE} and ground, respectively. They are designed to maximize sensitivity to adherent bacteria on the given pixel area [Fig. 2(a)], fixed by the underlying readout circuit to 14 μm × 16 μm (see Section III-C). Gaps $d_e = 2$ μm, widths $w_e = 2$ μm and lengths $L_e = 14$ μm provide a maximal active area, a regular pattern and enough place to let bacteria bind between microelectrodes, where electric field is maximal. The capacitance C_{IDE} of these electrode configuration is impacted mainly by the interaction between the electrode at V_{IDE} and its counterpart at ground, but also by ground electrodes of neighborless pixels which give rise to fill factors larger than 100%.

Another key design parameter is the insulating layer covering these electrodes and protecting them from electrochemical corrosion in biological buffers. Indeed, the electrical equivalent model of one pixel [Fig. 2(b)] shows that the impedance must take into account the insulator capacitance C_{ins}, the dielectric interconnects capacitance C_{ox}, the transistor terminal capacitance C_{stray} and the electrical double layer (DL) capacitance C_{DL} in addition to the electrolyte capacitance C_{sol} and resistance R_{sol}. Following 2D approximations are given [24]:

$$C_{sol} \simeq \frac{\epsilon_{r,sol}\epsilon_0}{d_e} \cdot A_e \tag{4}$$

$$R_{sol} \simeq \frac{d_e}{\sigma_{sol}} \cdot A_e^{-1} \tag{5}$$

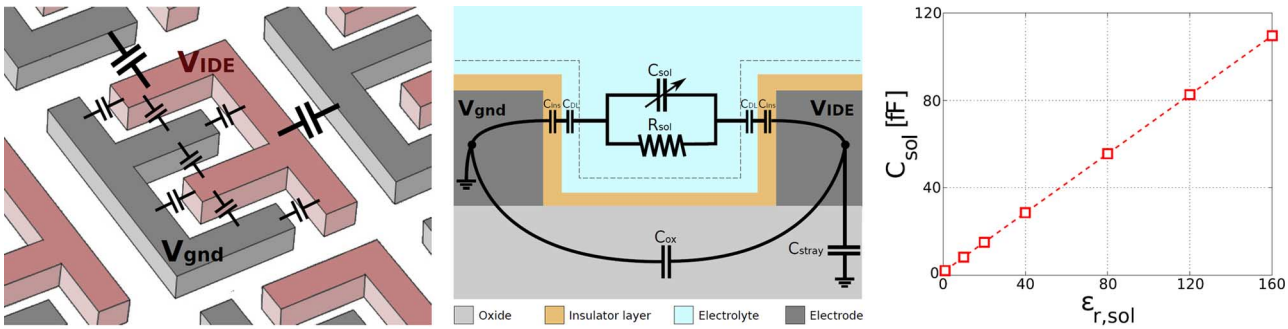

Fig. 2. Sensing part of the pixel. (a) 3D representation of the last metal layer (M5) of one pixel with the neighborless pixels highlighting the concerned capacitances. (b) 2D schematic cross-section of adjacent electrodes with their equivalent electrical circuit. (c) Simulation results of the dependence of capacitance $C_{ox} + C_{sol}$ with the solution relative permittivity $\epsilon_{r,sol}$, based on the 3D representation of Fig. 2(a).

$$C_{ins} \simeq \frac{\epsilon_{r,ins}\epsilon_0}{t_{ins}} \cdot A_e \tag{6}$$

$$C_{DL} \simeq \frac{\epsilon_{r,sol}\epsilon_0}{\lambda_D} \cdot A_e \tag{7}$$

with $d_e = 2\ \mu$m the electrode gap, $t_{ins} = 25$ nm the insulator thickness, $A_e \approx (h_e + w_e/2)L_e$ the electrode area, $h_e = 1.8\ \mu$m the electrode thickness, $\epsilon_{r,sol} = 80$ the electrolyte relative permittivity, $\epsilon_{r,ins} = 9$ the insulator relative permittivity, $\sigma_{sol} = 1.8$ mS/m the electrolyte conductivity, $\lambda_D \simeq 24$ nm the Debye length and ϵ_0 the vacuum permittivity. These values consider an Al_2O_3 insulator layer and a phosphate-buffered saline (PBS) electrolyte diluted 1:1000 by volume in deionized (DI) water. Since the sensing principle is based on linear change of C_{sol} with the number of adherent bacteria [10], [25], it is important to quantify the reduction of sensitivity caused by lumped elements R_{sol}, C_{ins}, C_{DL}, C_{ox} and C_{stray}. The resistance R_{sol} does not perturb the capacitance conversion of C_{sol} because the corresponding time constant is evaluated to $\tau \simeq \epsilon_{r,sol}\epsilon_0/\sigma_{sol} = 400$ ns, which is far larger than the 25 ns clock period between V_{c1} and V_{c2}. Furthermore, the ratio $C_{DL}/C_{ins} \simeq \epsilon_{r,sol}/\epsilon_{r,ins} \cdot t_{ins}/\lambda_D \simeq 9.3$ shows that C_{ins} dominates C_{DL} in series, while $(C_{ins}/2)/C_{sol} \simeq \epsilon_{r,ins}/\epsilon_{r,sol} \cdot d_e/2t_{ins} \simeq 4.5$ demonstrates that C_{ins} cannot be neglected in series with C_{sol}. By assuming C_{ox} and C_{stray} far smaller than C_{sol} in parallel (see next paragraph and Section III-C for justification), the IDE capacitance C_{IDE} can be approximated to

$$C_{IDE} \simeq (2C_{ins}^{-1} + C_{sol}^{-1})^{-1} \simeq 0.82 \cdot C_{sol}. \tag{8}$$

To accurately estimate C_{sol}, 3D finite-element simulations of the electrode design in Fig. 2(a) were performed with Comsol Multiphysics®, by assuming no insulator and double layers. It highlights the following linear dependence of C_{sol} with $\epsilon_{r,sol}$ [Fig. 2(c)]: $C_{sol} = 2$ fF $+ 0.68$ fF $\cdot\ \epsilon_{r,sol}$. In typical electrolyte featuring $\epsilon_{r,sol} = 80$, the solution capacitance is then equal to $C_{sol} = 55.6$ fF. By setting $\epsilon_{r,sol} = 0$, the capacitance corresponds to C_{ox} and is equal to 2 fF, which is far smaller than C_{sol}, as expected. The cell constant K_{cell} is equal to $(\epsilon_0\epsilon_{r,sol})/C_{sol} = 127\ \text{cm}^{-1}$, giving the following value for the solution resistance: $R_{sol} = K_{cell}\sigma_{sol}^{-1} \simeq 7\ \text{M}\Omega$.

TABLE I
TRANSISTOR SIZING

Transistor	Type	(W/L) sizing
M_{C1}	NMOS high-V_{th}	(0.58 μm/0.24 μm)
M_{C2}	NMOS high-V_{th}	(0.58 μm/0.24 μm)
M_{INIT}	NMOS high-V_{th}	(0.58 μm/0.24 μm)
M_T	NMOS high-V_{th}	(5.5 μm/5.5 μm)
M_R	NMOS high-V_{th}	(0.58 μm/0.24 μm)
M_{BUF}	NMOS low-V_{th}	(3.86 μm/0.5 μm)
M_{SEL}	NMOS low-V_{th}	(0.58 μm/0.5 μm)
C_D	PMOS capacitance (100 fF)	(3.95 μm/3.95 μm)
M_B	NMOS high-V_{th}	(0.8 μm/2 μm)
M_{SHR} - M_{SHS}	NMOS high-V_{th}	(0.58 μm/0.7 μm)
M_{BUFR} - M_{BUFS}	PMOS high-V_{th}	(9.5 μm/1 μm)
M_{SELR} - M_{SELS}	PMOS high-V_{th}	(0.58 μm/0.35 μm)
C_{SHR} - C_{SHS}	NMOS capacitance (300 fF)	(6.82 μm/6.82 μm)
M_{BR} - M_{BS}	PMOS normal-V_{th}	3 x (13 μm/12 μm)

Available values of threshold voltages V_{th0} in the 0.25-μm CMOS technology: NMOS: 60 mV, 180 mV and 480 mV; PMOS: 290 mV and 600 mV.

C. Design of the Pixel Circuit

The charge sharing circuit is designed to obtain a gate voltage V_{gT} proportional to C_{sol}, free of non-linearities and independent of C_{ins}, C_{DL} and R_{sol} [(see (1)]. Switches M_{C1}, M_{C2} and M_{INIT} are high-V_{th} transistors with minimized widths and channel lengths to reduce clock feedthrough and charge injection. Based on sizes given in Table I, the stray capacitance C_{stray} has a simulated value of 4 fF, which is far smaller than the solution capacitance $C_{sol} = 55.6$ fF. The transition t_{ov} between V_{c1} and V_{c2} must be sufficiently small to have a proper and stable operation at $\sigma_{sol} \leq 0.05$ S/m [Fig. 3(a)]. In this work, t_{ov} was fixed to the clock period (25 ns) to limit the V_{gT} drop around $\sigma_{sol} \simeq 0.01$ S/m below 15% of the V_{gT} value at $t_{ov} = 5$ ns and to provide a sufficient sensitivity at $\sigma_{sol} < 0.05$ S/m. At $\sigma_{sol} > 0.05$ S/m, the insulator capacitance dominates ($C_{IDE} \simeq C_{ins}/2$) making

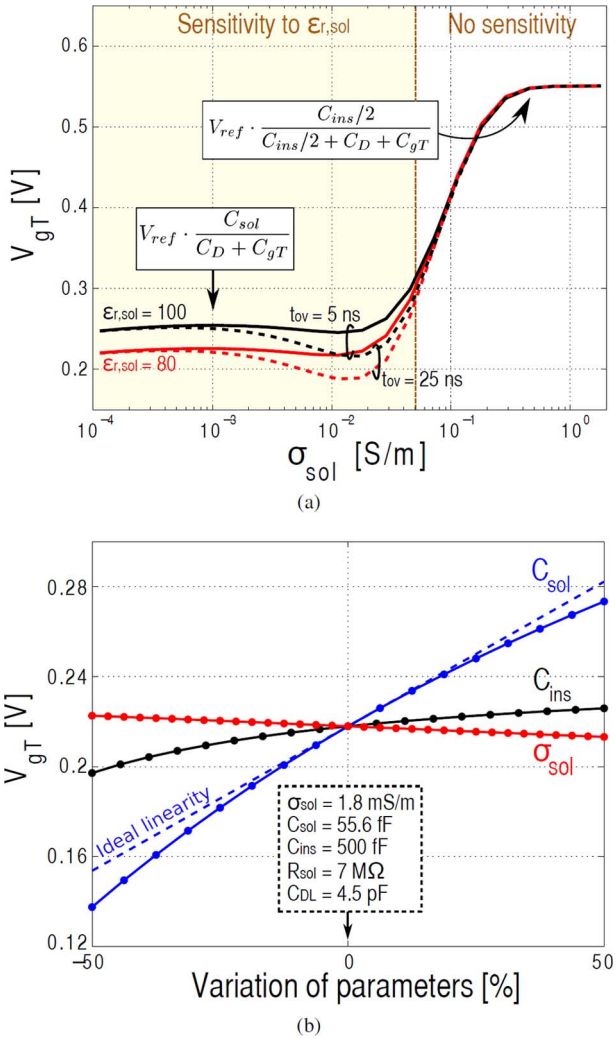

Fig. 3. SPICE simulation results of (a) the impact of the electrolyte conductivity σ_{sol} on the gate voltage V_{gT} of M_T for several values of t_{ov} and $\epsilon_{r,sol}$ and (b) the impact of variation of C_{sol}, C_{ins} and σ_{sol} (thus impacting R_{sol} and C_{DL}) within ±50% of their nominal value on V_{gT}. V_{ref} is fixed at 0.9 V and the lumped elements shown in Fig. 2(b) are used in SPICE.

$V_{gT} \simeq V_{ref} \cdot C_{ins}/2/C_{ins}/2 + C_D + C_{gT}$ from (1). Consequently, V_{gT} does not change with $\epsilon_{r,sol}$ anymore, whatever the value of t_{ov}. Around the nominal operating point where $\sigma_{sol} = 1.8$ mS/m, $\epsilon_{r,sol} = 80$ and $\epsilon_{r,ins} = 9$, V_{gT} predominantly and linearly depends on C_{sol}, featuring a maximum non-linearity of 10% at ±50% of its variation [Fig. 3(b)]. Furthermore, V_{gT} is almost insensitive to variations of C_{ins} and σ_{sol}, featuring maximal deviations of 9% and 2% on V_{gT}. The sensing principle is thus mainly impacted by dielectric medium properties, and immune to unexpected corrosion of the insulator layer [26]or ionic contamination of the electrolyte buffer [10], both being inexistent in this work anyway.

To provide the high linearity between V_{gT} and C_{sol}, the capacitance C_D has been chosen constant and sufficiently larger than C_{sol}, but with moderation to limit degradation of the pixel area and sensitivity [see (1)]. A MIM capacitance cannot be used since microelectrodes are patterned in the last metal layer. Since the gate voltage V_{gT} is typically small to place M_T in weak inversion, a PMOS capacitor was used and its variation does not exceed 1.5% as V_{gT} spans from 0 to 0.5 V, since it operates in strong inversion. A 3.95 μm × 3.95 μm size provides a 100 fF capacitance C_D, therefore two times larger than C_{sol}. In addition, M_T is also designed with large width and channel length $(W/L) = (5.5\ \mu\text{m}/5.5\ \mu\text{m})$ to increase its gate capacitance C_{gT} to 45 fF, reduce its Early effect and reduce the local mismatch on I_{dT}, detrimental for the FPN. V_{ref} is chosen to boost S_r, with the experimental procedure described in Section IV-C.

The pixel source follower is designed to load a column bus capacitance $C_{col} \simeq 1$ pF in 6 clock periods (150 ns) and consists of a buffer transistor M_{BUF}, a row switch M_{SEL} and a biasing transistor M_B included in a column amplifier. For noise and timing constraints, the g_m/I_d of M_{BUF} is maximized to a high value of 22 V^{-1} (weak inversion) thanks to a low-V_{th} feature. To have a settling error smaller than the 1-mV resolution of the off-chip ADC, the charging time t_{ch} must be 8 times larger than the time constant $\tau_{ch} = C_{col}/g_m$. Since t_{ch} is limited to 6 clock periods (i.e., 150 ns) and $C_{col} \simeq 1$ pF, the g_m value of M_{BUF} is fixed to 60 μS and the drive current therefore to 2.7 μA. Based on the g_m/I_d method [27], the biasing voltage V_b and the (W/L) ratio are found to be 0.7 V and 7.7, respectively, which results in sizes mentioned in Table I by minimizing the channel length for reduction of the pixel area. For the design of M_B, high-V_{th} NMOS is chosen with $g_m/I_d = 7.3\ \text{V}^{-1}$ (moderate inversion) to reduce noise. Giving $(W/L) = 0.4$, a large L is chosen to reduce the column FPN. Because of the non-zero body source voltages of M_{BUF} and M_{SEL}, the source follower suffers from a non-linearity of 3% per unit voltage as V_{pix} ranges from 0.5 V to 2 V.

D. Design of the Column Amplifier Circuit

The storage of the reset and signal values are ensured by large capacitances C_{SHR} and C_{SHS}. Designed to fill the column amplifier width with a squared shape, the capacitances have a value of 300 fF that enable only 3 mV shift after 100 μs of storage, thanks to high-V_{th} transistors M_{SHR} and M_{SHS} featuring low leakages in OFF state.

The two source followers are identically sized and next developments are only focused on the part storing the reset value. It consists of three transistors M_{BUFR}, M_{SELR} and M_{BR}, which have large widths and channel lengths to minimize the column-based FPN. It is crucial for M_{SELR} to be high-V_{th} in order to reduce its drain leakage current and avoid the drain voltage of M_{BUFR} to increase with time, and perturb the storage node by capacitive coupling. The same methodology as the source follower of Section III-C is used to size M_{BUFR} and M_{BR} and provides biasing voltage $V_{br} = 1.55$V. However, the body of PMOS transistors is connected to the source to limit non-linearity from body effect, which was not possible in pixel for size constraint due to triple well. With an output load capacitance approximated to 100 pF, the maximal charging time t_{read} is 8 μs. With the sizes provided in Table I, the source follower achieves a non-linearity of 6.9% per unit voltage from 0 to 1.4 V.

IV. Experimental Validation

In this section, experimental tests performed with the fabricated chip are detailed. First, the physical implementation of the chip including post-process steps is explained in Section IV-A,

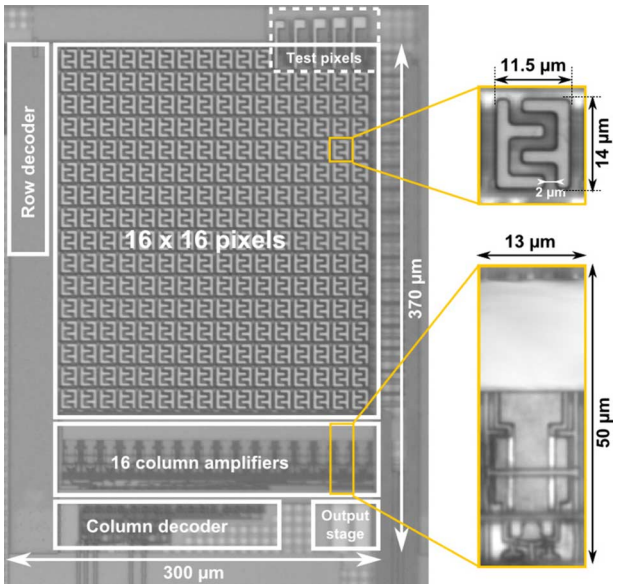

Fig. 4. Chip microphotograph with pixel and column amplifier zoom.

as well as the measurement setup. Then in Section IV-B, functionality of the capacitive array is confirmed at dry condition and with basic solutions without bacterial cells. Finally, the real-time detection of bacterial cells is demonstrated in Section IV-C.

A. Physical Implementation and Measurement Setup

A 16 × 16 capacitive biosensor array was fabricated in an industrial 0.25-μm 2.5-V multi-V_{th} 1 P5M Mixed-Signal CMOS process, comprising a 1.8 μm-thick Al 99.5%/Cu 0.5% last metal layer (M5) for sensing parts. As shown in Fig. 4, five test pixels were included at the end of the first line and have MIM capacitances of known values, ranging from 25 fF to 65 fF by step of 10 fF, instead of pixel microelectrodes. The CMOS dies were not covered by the thick SiO_2/Si_3N_4 passivation layer and were encapsulated in open-top CQFP160 packages. The wirebonds were covered by UV-cured epoxy resin to avoid contact with liquid during experiments. As characterized by ellipsometry, a 25 ± 0.25 nm-thick Al_2O_3 layer was deposited by plasma-enhanced atomic layer deposition (PE-ALD) at room temperature with trimethylaluminum (TMA) and oxygen as precursor. The argon flow through plasma source was 200 sccm and the oxygen flow for the plasma step was 30 sccm during 20 sec.

The open-top CQFP160 packages were soldered on slave printed circuit boards (PCB), each successively mounted in a master PCB to enable multiple purpose measurements. Digital signals were generated by the National Instruments® (NI) PXI-6552 card while analog output signals from the chip were converted to digital signals by the NI PXI-5105 card. Supply and biasing voltages were provided by the N6715B and K2400 equipments. All the setup and data acquisition were controlled through LabVIEW.

B. Circuit Functionality

At dry condition, the readout time t_{read} was first ajusted to 20 μs to let V_{outr} and V_{outs} achieve their steady state values. The time t_{ov} was fixed to the clock period (25 ns), while t_{int} to

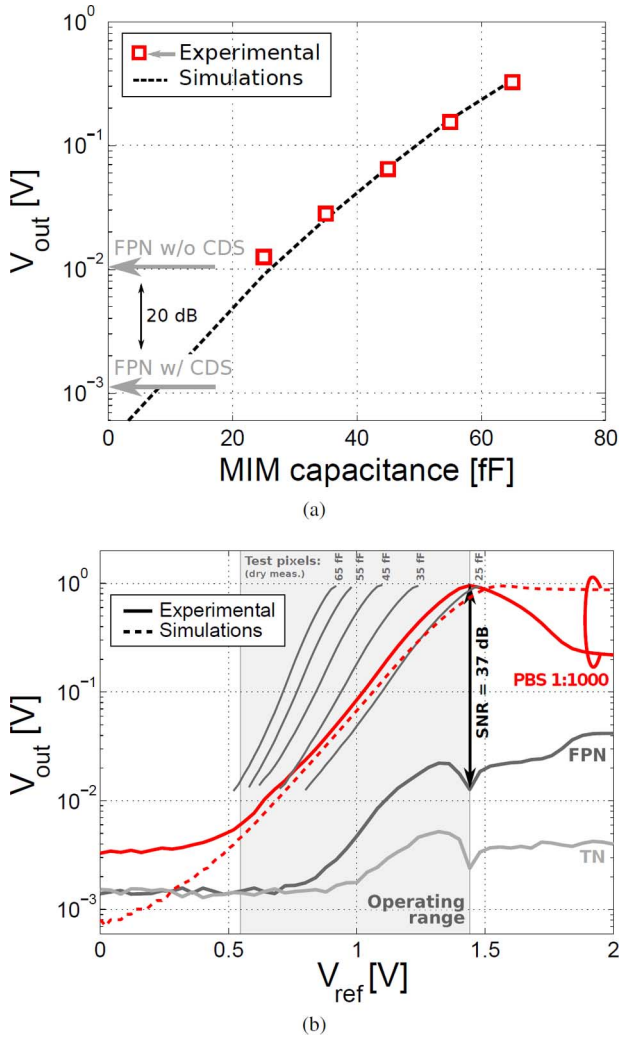

Fig. 5. (a) Experimental and simulated characteristics of the output voltage V_{out} of test pixels versus their MIM capacitance values at $V_{ref} = 0.8$ V and at dry condition, showing the FPN values with and without CDS. (b) Experimental and simulated mean pixel output V_{out} versus V_{ref} in PBS 1:1000 with corresponding measured FPN and temporal noise (TN) levels, including comparison with measured characteristics of test pixels at dry condition. SPICE simulations account for the model in Fig. 2(b).

2 μs for dynamic range (DR) purposes. Test pixels with known MIM capacitance values ranging from 25 fF to 65 fF present output voltages V_{out} with exponential dependence on MIM capacitances [as expected from (3)] and that perfectly match post-layout simulations at dry condition [Fig. 5(a)]. FPN levels at $V_{ref} = 0.8$ V with and without CDS were computed from the difference $V_{outr} - V_{outs}$ (3) and from the voltage V_{outs} only, respectively, on all except edge pixels. Using CDS demonstrates a FPN reduction by a factor 9, which is close to 20 dB of improvement [Fig. 5(a)]. The array consumes 29 μW at a frame rate of 37 frames per sec, corresponding to an energy efficiency of 3 nJ/(frame.pixel).

To validate sensing capabilities of all pixels, a 10 μL drop of PBS 1:1000 was pipetted atop the capacitive array and the package lid closed to avoid drop evaporation and to work under dark condition. The mean output voltage computed on all except edge pixels highlights three different regions of operation depending on V_{ref} [Fig. 5(b)]. At $V_{ref} < 0.6$ V, the output voltage

is dominated by parasitics and noise. From 0.6 V to 1.3 V (the operating range), M_T progressively goes from weak to strong inversion and provides a readable output voltage dependent on V_{ref} and C_{IDE} according to (1). Above 1.3 V, V_{out} strongly decreases as V_{outr} drops because of the large value of V_{gT}. At each V_{ref}, ca. 10 successive temporal measurements were acquired and FPN was computed as the standard deviation of the mean temporal values of each pixel, while the temporal noise (TN) as the average of the standard deviations obtained on successive temporal values of each pixel. As shown in Fig. 5(b), FPN and TN have close values and both increase with V_{ref}, because mismatch and noise from M_T in subthreshold are not compensated by CDS. For this reason, FPN in water [$\epsilon_{r,sol} = 80$, Fig. 5(b)] features larger values than FPN in air [$\epsilon_{r,sol} = 1$, Fig. 5(a)], where M_T is cut off thanks to small $C_{IDE} \simeq 2$ fF and does not add FPN. The measured noise figure follows the same evolution versus V_{ref} as that given by SPICE simulations, but is larger by a factor 3 due to the use of external ADC that adds uncorrelated noise of 1-mV characterized amplitude on V_{outr} and V_{outs}. The maximal signal-to-noise ratio (SNR), accounting for both FPN and noise, is shown to be 37 dB at $V_{ref} = 1.28$ V. By comparing the measured characteristics V_{out} versus V_{ref} of the different test pixels at dry condition, the slopes are different because of the different values of β expressed in (1). The larger the MIM capacitance, the larger the value of β and therefore the steeper the slope. In solution, the effective capacitance C_{IDE} is also slightly smaller than C_{sol} [see (8)], so that β is smaller compared to a fixed MIM capacitance of the same value. By considering this slope difference and comparing V_{out} values at the start of the subthreshold operation of $M_T (V_{ref} \simeq 0.7\,\text{V})$, C_{IDE} in PBS 1:1000 can be approximated to 40–45 fF [Fig. 5(b)], which is ca. 80% of the simulated C_{sol} value of (55 fF), as expected by (8). SPICE simulations including the IDE model of Fig. 2(b) confirms the good matching in the operating range.

To assess that pixel outputs depend on dielectric medium properties, the capacitive array was subject to several glycerol dilutions, featuring different relative permittivities characterized with a VNA (Agilent N5242A) connected to a dielectric probe (Agilent 85070E) at 419 MHz: 35.5, 55.6, 66.9, 73.5 and 81.6 for glycerol, glycerol 3:4, glycerol 1:2, glycerol 1:4 and DI water, respectively. These relative permittivity values can be considered as good approximations for DC relative permittivities, since dielectric dispersion occurs beyond 419 MHz. Within the operating range, the mean pixel output and its slope both increase for larger $\epsilon_{r,sol}$ [Fig. 6(a)] for the same reasons as test pixels. At fixed V_{ref}, V_{out} is shown to be exponentially dependent on $\epsilon_{r,sol}$ [Fig. 6(b)] and confirms (3). Since C_{sol} changes by 1 fF as $\epsilon_{r,sol}$ goes from 80 to 78.5, the sensitivity $S \triangleq \partial V_{out}/\partial C_{sol}$ computed around $\epsilon_{r,sol} = 80$ has a maximal value of 55 mV/fF at $V_{ref} = 1.36$ V. On the other hand, the relative sensitivity defined by (2) is identical for all $\epsilon_{r,sol}$ [Fig. 6(a)] and has a maximal value of 6.3%/fF at $V_{ref} = 1.24$ V. As expected, S_r is maximized in the subthreshold slope at estimated gate voltage $V_{gT} \simeq 0.3$ V, thus well beyond $\alpha = 42$ mV (cfr Section III-A and Appendix A). Since the noise at $V_{ref} = 1.36$ V has a value of 5 mV [Fig. 5(b)], the detection limit corresponding to five times the noise is evaluated to 450 aF. Accordingly, the dynamic range is evaluated to $20 \cdot \log_{10}(55.6\ \text{fF}/0.45\ \text{fF}) \simeq 42$ dB.

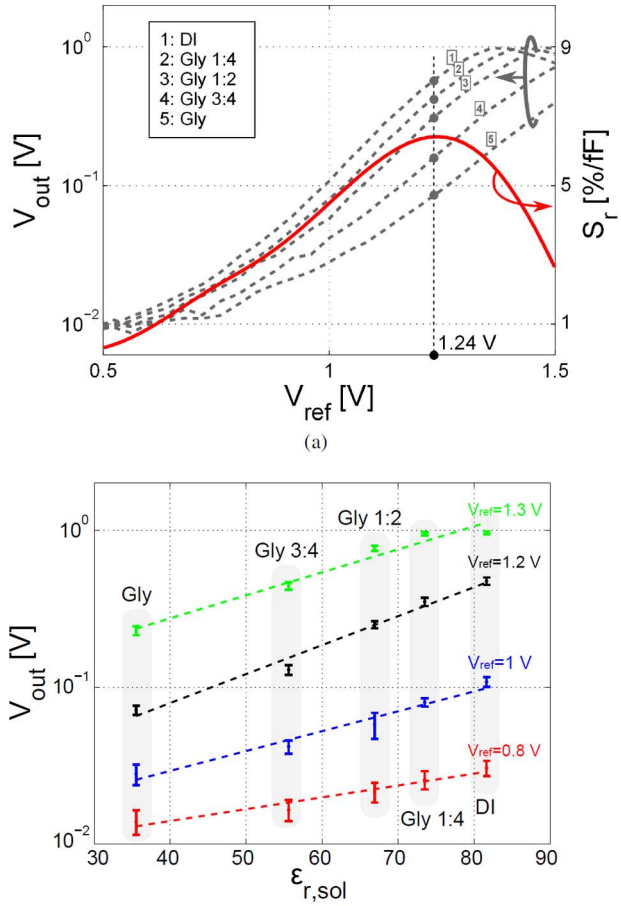

Fig. 6. Experimental dependence of V_{out} with (a) V_{ref} for several glycerol dilutions and with (b) the solution permittivity $\epsilon_{r,sol}$ of these dilutions for several V_{ref}, considering all except edge pixels for mean and standard deviation. For (a), the relative sensitivity S_r is also shown and is identical for all glycerol dilutions.

C. Sensing of Bacterial Cells

In this section, the response of the biosensor array to bacterial cells contained in a low-conductive buffer is investigated. In contrast to Section IV-B, all pixels are not supposed to give the same output voltage anymore, since bacterial cells can preferably adhere to some pixels. After cultivated on agar plates at 37°C overnight, one single colony of *S. epidermidis* ATCC 35984 was suspended in 50 mL of Tryptic Soy Broth (TSB) and incubated overnight at 37°C. Afterwards, the culture was centrifugated and bacterial cells were resuspended in PBS 1:1000, the reference buffer. This step was repeated two times. The bacterial concentration was evaluated to $5 \cdot 10^8$ CFU/ml by surface plate counting. The capacitive array was first measured under sterile PBS 1:1000 with V_{ref} spanning from 0 to 2.5 V. Then, a real-time experiment on the capacitive array was performed based on the following protocol. The reference

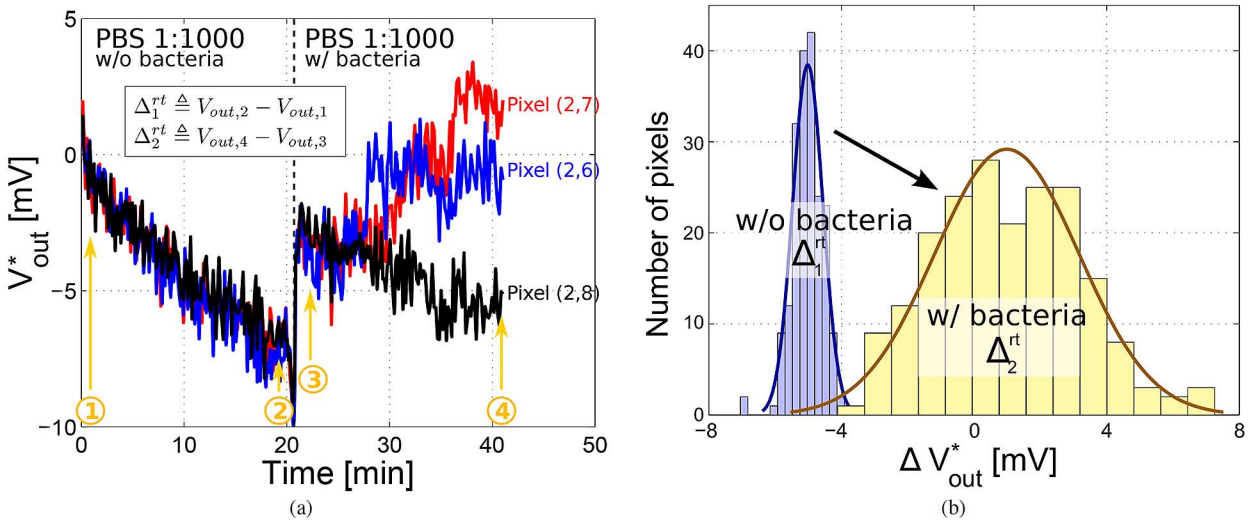

Fig. 7. Experimental biosensing of real-time *S. epidermidis* binding on the sensor surface. (a) Temporal evolution of the output voltages V^*_{out} of three different pixels, set identical at $t = 0$ s. (b) Statistical evolution of $\Delta_1^{rt} \triangleq V^*_{out,2} - V^*_{out,1}$ and $\Delta_2^{rt} \triangleq V^*_{out,4} - V^*_{out,3}$ on all pixels. V_{ref} is set to 1.06 V.

buffer, the bacterial solution and the reference buffer again were successively incubated on the array surface, 20 minutes each time with lid closed and under electrical measurements at $V_{ref} = 1.06$ V, a midrange value in the subthreshold slope. The chip surface was then dried and observed by optical microscopy to localize bacterial binding. Then, the capacitive array was re-measured in PBS 1:1000 with V_{ref} spanning from 0 to 2.5 V to find the best conditions achieving the maximal sensitivity with regards to the initial measurement. As the bacterial-covered surface can hardly be cleaned without damaging the array, the biochip was discarded after a single experiment to avoid any interference.

The temporal evolution of the three distinct pixel outputs (2,6), (2,7) and (2,8) during the two first incubation phases is described in term of $V^*_{out}(t) = V_{out}(t) - V_{out}(0)$ to suppress pixel mismatch and facilitate comparison [Fig. 7(a)]. During the first 20 min, the three pixel outputs present a similar drift of approximately 5 mV [Fig. 7(a)], occuring because of the slight drop evaporation. The voltage difference at times $[t_1, t_2] = [3, 19]$ min defines the shift $\Delta_1^{rt} \triangleq V^*_{out,2} - V^*_{out,1} = V_{out,2} - V_{out,1}$, which has a Gaussian distribution computed on all pixels with a -5-mV mean and 0.45-mV standard deviation. As the solution with bacterial cells is pipetted, the pixel values recover their initial levels instantaneously but each pixel presents different evolutions [Fig. 7(a)]. To quantify this, a second shift $\Delta_2^{rt} \triangleq V^*_{out,4} - V^*_{out,3} = V_{out,4} - V_{out,3}$ is defined with $t_3 = 24$ min and $t_4 = 40$ min, and features a broader distribution centered around 1 mV with a standard deviation of 2.2 mV [Fig. 7(b)]. Compared to Δ_1^{rt}, the mean value increased by 6 mV because bacterial binding induces an increase of pixel capacitances, as previously demonstrated in [10], [11], [25]. Indeed, the bacterial impedance is dominated by the large outer shell capacitance, thus increasing the global capacitance between electrodes [24]. The large dispersion of Δ_2^{rt} is due to the fact that all pixels do not have the same number of bacteria and that their positions affect the capacitance value [25].

To quantify the voltage shift per bacterium, the number of adherent bacteria on each pixel was estimated from microscope images taken after the real-time experiment. Bacterial cells appear black (type 1) or white (type 2) depending on their respective positions between or atop microelectrodes [Fig. 8(a)]. This distinction is important since the position of adherent bacterial cells slightly affect the capacitive shift [25]. Pixel outputs with the same number of bacteria can then exhibit non-negligible variability arising from these random bacterial positions. 3D simulations of the pixel represented in Fig. 2(a) demonstrates that both pixel capacitance and output voltage increase with the bacteria number N_b, but with a large variability [Fig. 8(c)]: $\Delta V_{out} \simeq (2.6 \pm 0.6\ \text{mV}) \cdot N_b$ and $\Delta C_{sol} \simeq (61 \pm 14\ \text{aF}) \cdot N_b$. Despite the exponential transfer function of M_T [see (1)], a linear dependence between the mean ΔV_{out} and N_b is observed because of the very small capacitance shifts ($< 1\%$ of the nominal value at $N_b < 10$). In these simulations, the signal-to-noise ratio (SNR) achieves a peak value of 13 dB at $N_b = 10$ showing that biological noise established in [25]and independent of V_{ref} strongly limits the biosensor performance. It is also confirmed that the relative sensitivity is strongly enhanced by the weak inversion of M_T, from 1% at the input capacitance level to 3.6% at the output voltage. Experimentally, since it was not possible to optically observe bacteria binding during the real-time incubation, only V_{out} measured for each V_{ref} before and after the bacterial incubation are compared. The maximal sensitivity to bacterial cells is obtained at $V_{ref} = 1.24$ V (data not shown), as expected from Fig. 6(a). The pixel output voltage V_{out} is shown to increase with the number of adherent bacterial cells [Fig. 8(b)], and presents the following dependence on N_b: $\Delta V_{out} \simeq -14.6\ \text{mV} + 2.18\ \text{mV} \cdot N_b$. The negative value at $N_b = 0$ is due to the slight difference in the electrical conductivity of the electrolyte between the initial and final wash, as it is very likely for low-conductive electrolytes ($\sigma_{sol} \simeq 1.8\ \text{mS/m}$). There is a good matching between experimental data and 3D simulations since the sensitivity to bacteria is fairly the same, i.e., 2.18 versus 2.6 mV/bacteria, respectively. Based on the sensitivity of 35.3 mV/fF at $V_{ref} = 1.24$ V (see Section IV-B), one bacterial cell is then represented by a capacitance increase of 62 aF, which is the same order of magnitude as in [10]. Since

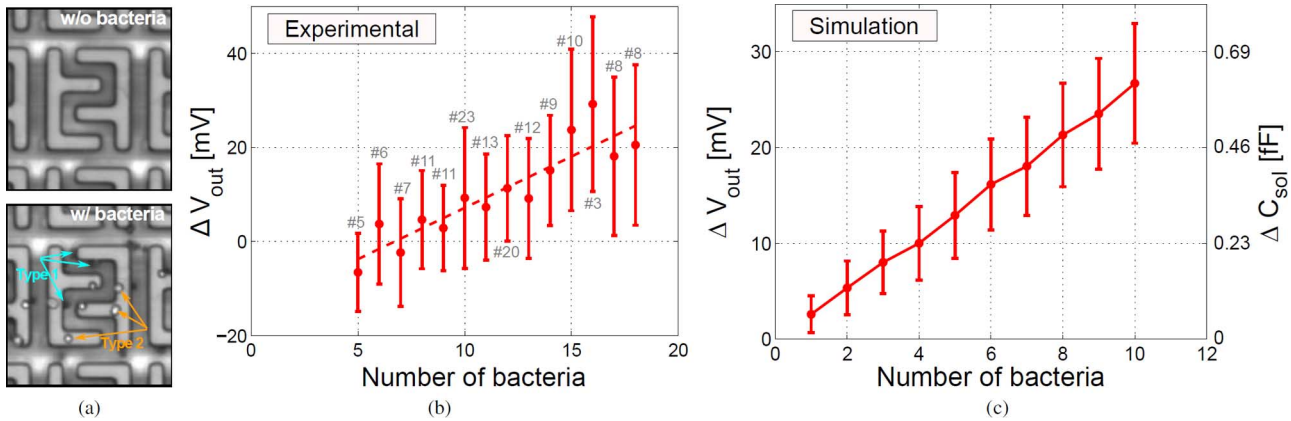

Fig. 8. Impact of the number of bacteria per pixel on the pixel output. (a) Microscope images of one pixel before and after the bacterial binding. Two types of adherent bacteria are found: type 1 corresponds to bacteria between electrodes, while type 2 corresponds to bacteria atop electrodes. (b) Experimental output voltage after wash versus the number of adherent bacteria, computed on all countable pixels of the array at the optimum $V_{ref} = 1.24$ s. The number of pixels used for each error bar is indicated by the symbol #. Edge pixels and pixels where the number of bacteria cannot accurately be estimated were discarded. (c) 3D simulation results of random bacterial deposition on the 3D structure of Fig. 2(a) at $V_{ref} = 1.24$ V. Each error bar is obtained by averaging 200 independent simulation results involving different bacterial positions.

TABLE II
CMOS CAPACITIVE BIOSENSORS FROM THE STATE OF THE ART

Ref.	Techno.	Supply	# sensors†	Sensor size	Sensor material	IC area	Principle	Biospecies	Medium	LoD	Power	Sensitivity	Input range
[12]	0.35-μm CMOS	3.3 V	**320 x 320**	20 μm x 20 μm	Al/CMOS passiv.	NA	18-T C2V (D): SC + ADC	10 μm beads	280 mM mannitol	21 aF (Single bead)	NA	345 mV/fF 145 mV/bead	NA
[13]	0.5-μm CMOS	5 V	**8 x 16**	200 μm x 200 μm	Au	28.8 mm^2	26-T C2f (D): CB-oscillator	DNA	0.3 M NaCl	NA	NA	23 Hz/pF @ 7.5 kHz @ 330 pF	330 pF - 10 nF
[22]	0.5-μm CMOS	3 V	28	20 μm x 20 μm	Al/CMOS passiv.	0.16 mm^2	(>8)-T C2V (ND): Charge sharing	Cancer cells	Growth medium	$\sim$ 5 fF (10^5 cells/mL)	NA	NA	NA
[19]	0.5-μm CMOS	3 V	**6 x 6**	NA	Al/CMOS passiv.	3 mm^2	4-T C2V (D): CBCM	-	-	15 aF (NA)	2.6 mW	200 mV/fF	$\pm$25 fF
[20]	0.18-μm CMOS	1.8 V	1	100 μm x 100 μm	Al/CMOS passiv.	2 mm^2	(>25)-T C2V (D): CBCM	*E. coli*	LB medium	NA (10^7 CFU/mL)	NA	255 mV/fF††	NA
[14]	0.35-μm CMOS	NA	**16 x 8**	170 μm x 80 μm	Au	10 mm^2	C2f (ND): TIE	DNA	PBS-Tween	5 pF (10 nM)	NA	NA	5 pF - 5 nF
[15]	0.35-μm CMOS	3.3 V	**10 x 10**	100 μm x 100 μm	Au	4 mm^2	32-T C2V (ND): TIA + coher.	DNA	4xSSC	10 nS (10^5)	85 mW	NA	NA
[17]	0.35-μm CMOS	NA	**5 x 5**	200 μm x 200 μm	Al/SiO_2	NA	(>9)-T C2f (ND): CB-oscillator	Neurotrans. polydop.	NA	NA (0.1 fM)	NA	21 kHz/fF @ 4.9 MHz @ 123 fF	12 fF - 700 fF
[28]	0.18-μm CMOS	3.3 V	**3 x 3**	100 μm x 100 μm	Al/CMOS passiv.	1.8 mm^2	4-T C2V (ND): CBCM	0.5-2μm beads	DI water	1fF (NA)	NA	10 fF/mV	NA
[16]	0.13-μm CMOS	1.2 V	**4 x 4**	200 μm x 300 μm	Au	1.68 mm^2	FRA (ND)	DNA	PPB with $Fe(CN)_6^{3/4-}$	0.42 fF (NA)	1.7 mW	NA	0.13 fF - 53 pF
[18]	0.35-μm CMOS	NA	**8 x 8**	100 μm x 100 μm	Al/SiO_2	NA	(>9)-T C2f (ND): CB-oscillator	10-μm beads	Air	2.5 fF (Single bead)	NA	223 kHz/fF @ 5.2 MHz @ 23 fF	NA
[11]	0.25-μm CMOS	2.5 V	1	220 μm x 230 μm	Al/Al_2O_3	0.05 mm^2	(>25)-T C2f (ND): CB-oscillator	*S. epi-dermidis*	PBS	10 fF (10^7 CFU/mL)	29 mW	11 kHz/fF @ 254 MHz @ 17.5 pF	NA
This work	0.25-μm CMOS	2.5 V	**16 x 16**	14 μm x 16 μm	Al/Al_2O_3	0.1 mm^2	7-T C2V (ND): Charge sharing	*S. epi-dermidis*	PBS 1:1000	450 aF** ($\sim$ 7 bact.)	29 μW	55 mV/fF* 2.2 mV/bact**	0.45fF -57 fF†††

NA: Not Available, CBCM: Charge-base capacitance measurement, CB: Charge-based, TIA: Transimpedance amplifier, TIE: Triangular impedance extraction, FRA: Frequency Response Analysis, C2V: Capacitance-to-voltage conversion, C2f: Capacitance-to-frequency conversion, ADC: Analog-to-digital conversion, SC: Switched-capacitors, D: Differential, ND: Non-differential, PBS: Phosphate buffered saline, PPB: Potassium phosphate buffer, SAM: Self-assembled monolayer, DR: Dynamic range, SNR: Signal-to-noise ratio, T: Transistor,
†: Arrays are in bold, ††: Only simulated value, †††: Tunable by t_{int} and V_{ref}, *: Around $\epsilon_{r,sol} = 80$ and at $V_{ref} = 1.3$ V, **: Around $\epsilon_{r,sol} = 80$ and at $V_{ref} = 1.06$ V.

the detection limit is 450 aF, the minimal detectable number of bacteria is approximately 7.

V. COMPARISON WITH RELEVANT WORKS

A comparison of performances from relevant CMOS capacitive biosensors is provided in Table II. Among biosensor arrays, our work is the first to focus on bacterial detection, while others deal with protein [17], DNA [13]–[16] and cells/beads [12], [18], [28]. In particular, [19] only shows functionality with on-chip capacitances, and not in biological solutions. Contrasting with these works, a more advanced CMOS technology (0.25 μm) and smaller pixels (16 μm × 14 μm) were required to enhance the sensitivity to bacteria without using differential measurements. For the same reason, miniaturized interdigitated electrodes with micrometer gap (2 μm) were used instead of single squared/disk electrodes. Similarly to [11], [17], [18], a thin passivated layer was post-processed on the last CMOS metal layer to protect it from corrosion. As in [11], the thickness (25 nm) was one order of magnitude smaller than in [17], [18] ($\sim$ 300 nm) to boost the sensitivity.

While most work used differential measurements to boost the sensitivity [12], [13], [19], [20], an innovative gain stage in subthreshold region was included along with a charge sharing capacitance-to-voltage conversion within the pixel to enlarge the sensitivity by a factor 4. Compared to the best reported limit of detection $\sim$ 20 aF [12], [19], the value achieved by this work is one order of magnitude larger (450 aF) but obtained without differential or pseudo-differential architectures. For the same reason, the sensitivity (55 mV/fF) is 4 to 5 times smaller as well compared to the best reported ones. However, the pixel size ($14\ \mu\mathrm{m} \times 16\ \mu\mathrm{m}$) and power consumption ($29\ \mu\mathrm{W}$) are the smallest and then provide benefits in term of IC area, costs and portability. Finally, thanks to the non-differential circuit, the design of this capacitive biosensor array can still be scaled in more advanced technology to eventually achieve single bacterial detection. The selectivity can also easily be provided by functionalization of the Al_2O_3 surface using antibodies [29] or by using lytic enzymes in volume [10].

VI. Conclusion

The design and fabrication of a 16×16 capacitive array in a $0.25\ \mu\mathrm{m}$ mixed-signal CMOS process has been reported towards single bacterial detection. Each pixel features two miniaturized interdigitated electrodes and a readout circuit based on the charge sharing principle that enables a linear capacitance-to-voltage conversion. To boost the bacterial sensitivity without differential measurements, a gain stage consisting of a single transistor operating in the subthreshold region was added after the linear capacitance to voltage conversion. Thanks to the non-differential architecture, the capacitive array offers possibilities for miniaturization and functionnalization. Experimental results demonstrate excellent matching with simulations, and confirm the sensing principle based on medium dielectric properties, featuring a maximal sensitivity of 55 mV/fF and a detection limit of 450 aF. As *S. epidermidis* bind on pixels in real-time, their output values were shown to be correlated to the number of adherent bacteria on each pixel. Each bacterial cell was shown to induce a 62 aF capacitance shift, corresponding to 2.18 mV in output.

Appendix
Linear Versus Exponential Sensitivity

Let A_{in} be a quantity subject to variation and A_{out} its value through a transfer function, either linear $A_{out}^{lin} = KA_{in}$ or exponential $A_{out}^{exp} = K\exp(A_{in}/\alpha)$, with fixed-value constants K and α. For a change ΔA_{in}, the respective relative sensitivities in linear and exponential modes are respectively

$$S_{r,lin} \triangleq \frac{1}{A_{out}^{lin}} \cdot \frac{\partial A_{out}^{lin}}{\partial A_{in}} = \frac{1}{A_{in}} \tag{9}$$

$$S_{r,exp} \triangleq \frac{1}{A_{out}^{exp}} \cdot \frac{\partial A_{out}^{exp}}{\partial A_{in}} = \frac{1}{\alpha}. \tag{10}$$

Consequently, the following relationship is obtained: $S_{r,exp} = (A_{in}/\alpha) \cdot S_{r,lin}$. The exponential relative sensitivity $S_{r,exp}$ is then always larger than $S_{r,lin}$ if $A_{in} > \alpha$.

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