A Double-Side CMOS-CNT Biosensor Array With Padless Structure for Simple Bare-Die Measurements in a Medical Environment

Jinhong Ahn, Sang Hoon Hong, and Youngjune Park, *Member, IEEE*

***Abstract*—This paper presents a double-side CMOS-carbon nanotube (CNT) sensor array for simple bare-die measurements in a medical environment based on a 0.35 μm standard CMOS process. This scheme allows robust measurements due to its inherent back-side rectifying diodes with a high latch-up resistance. In particular, instead of using pads, only two contact metal structures: a wide ring structure around the sensor area on the front side and a plate structure at the backside are used for both power and single I/O line. The back-side rectification is made possible by creating VDD and VSS through the back-side and front-side, respectively. The single I/O line is conditioned such that it doubles as either the power source or the ground, depending on whether the chip is face down or face up. A modified universal asynchronous receiver/transmitter (UART) serial communication scheme with pulse based I/O signal transmission is developed to reduce the power degradation during the signaling intervals. In addition, communication errors and I/O power dissipation for the receiver path are minimized by using level sensitive switch control and double sampling difference amplifier. In order to implement these special functions, a controller chip with a special I/O protocol is designed. Using this controller chip, issuing commands and receiving data can both be performed on a single line and the results are flexibly measured through either the backside or the front side of the chip contacts. As a result, a stable operation of under 150 mW maximum power at 2 MHz data rate can be achieved. The double-side chips with 32 $\times$ 32 and 64 $\times$ 64 sensor arrays occupy areas of 1.9 $\times$ 2.3 mm^2 and 3.7 $\times$ 3.9 mm^2, respectively.**

***Index Terms*—Backside rectification, bare-die measurement, biosensor array, CMOS, carbon nanotube (CNT), controller, double-side, flippable chip position, level sensitive switch control, medical, pulse communication, universal asynchronous receiver/transmitter (UART).**

Manuscript received August 20, 2015; revised October 15, 2015; accepted November 11, 2015. This work was supported by the Center for Integrated Smart Sensors (CISS-2012054186) and the National Research Foundation (NRF-2012-0009555), funded by the Ministry of Science of Korea. This paper was recommended by Associate Editor D. Ham.

J. Ahn was with Seoul National University, Seoul 151-742, Korea. He is now with Duality Inc., Daejeon 306-802, Korea (e-mail: jinhongahn@ snu.ac.kr).

S. H. Hong is with the Department of Electronics and Radio Engineering, Kyung Hee University, Yongin 130-701, Korea (e-mail: daniel@khu.ac.kr).

Y. Park is with the Department of Electrical Engineering, Seoul National University, Seoul 151-742, Korea (e-mail: ypark@snu.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2015.2500911

I. Introduction

CMOS sensors using nanomaterials on the surface as electrical signal generators are very effective for early detection and adequate treatment of diseases. Among the nanomaterials, carbon nanotube (CNT) is an ideal biosensor material because it has the smallest diameter ($\sim$1 nm) directly comparable to the size of biomolecules. One-dimensional (1-D) structure of carbon nanotubes (CNTs) allows signals to be propagated in a confined 1-D space, making them extremely sensitive to electrical and chemical changes in their immediate environments [1], [2]. A drawback of sensors using a single CNT is that its electrical properties are hard to control. For example, the energy gap of a nanotube is dependent on the tube diameter and the chiral vector, which implies very high variability of electrical properties. Recently, a new CNT-based electrical DNA biosensor system was reported, which consists of gold (Au) nanoparticle-decorated CNT network on top of concentric Au electrodes [3], [4]. Fig. 1 shows the biosensor's sensing mechanism. Carbon Nanotube Network Field-Effect Transistors (CNNFETs) were made by using the CNT network deposited on the concentric electrodes and in-between, to form an electrical channel of circular shape between the island electrode and the common enclosing one. The Au nanoparticle on the CNT network can be used as a substrate or a linker for biomolecular sensor application by attaching probe molecules with thiol functional group. In particular, the agglomeration process during Au deposition also provides better adhesion between the CNT network and the chip substrate and prevents the delamination of CNTs during soaking and/or storage in solution.

To form highly uniform and large-area CNT networks, a wafer dip-coating method, which is based on fluid-dynamic phenomena such as capillary condensation and surface tension is used [5]. However, to prevent electrical shorts between bonding pads, very complicated area-selective CNT coating processes are required [6], [7]. It is reported that if the ordinary CMOS photo and etch processes are used to remove the CNTs around the pad area, the complex surface structure of nanomaterials makes the removal of photoresist residues in the sensor area very difficult even through an extensive cleaning processes. This unwanted contamination due to the photo and etch process reduces the sensitivity of nanomaterial sensors significantly [8]. Furthermore, chip packaging process, such as wire bonding, chip passivation against reactions to the wire,

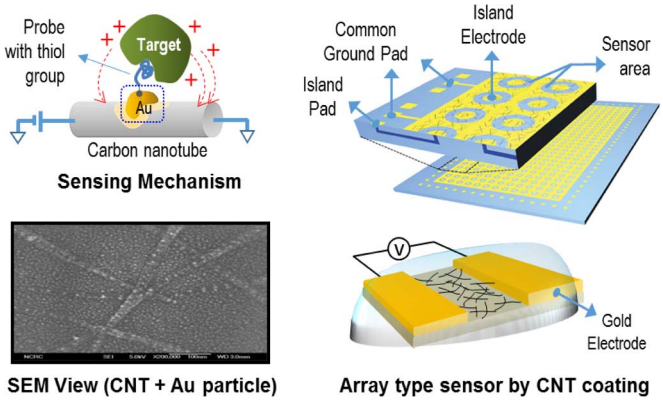


Fig. 1. Sensing mechanism and structure of CNT coated biosensor array.

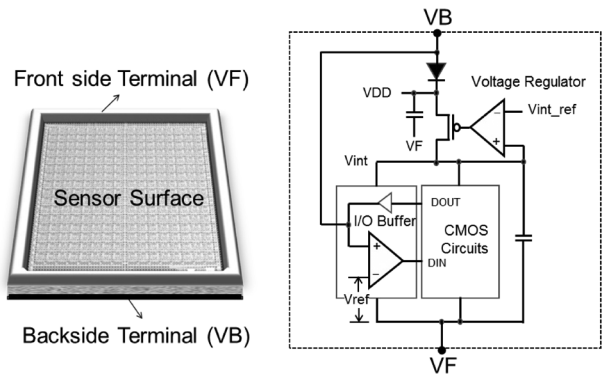


Fig. 2. Conceptual view of the 2-terminal padless sensor chip.

and microfluidic channels on the chip, etc., should be carefully applied [9].

Double-side chips can be a solution for these problems since it does not have pads on the surface and directly measurable without packaging. A double-side chip using Through-Silicon-Via process for RFID was reported, where a Silicon-on-Insulator wafer is used to remove the latch-up phenomenon [10]. However, for medical applications, which are mostly one-time usages, more cost-effective solutions are desired.

Fig. 2 shows the conceptual view of a flipped padless sensor chip. A flipped chip implies front-side of the chip face down on an electrically connected conductor. A padless chip is a 2-terminal device with double sided metal contacts. One terminal is a front-side metal, which can be a wide ring structure around the sensor area for sensor application, or a plate structure covering the whole chip area, and the other terminal is a backside metal, which is a plate structure formed by the backside metal coating for both power and I/O line. In this chip, one of the power terminals is the front-side metal, which acts as the ground, and the source power is extracted at the other terminal from "high" state of I/O line signals using the rectifier and the voltage regulator from the backside.

Fig. 3 shows the overview of the sensor preparation and the medical application procedure. A double-sided ID chip can be used for a wide variety of applications to label, track, and authenticate items in the clinical bioassays [11], [12]. By integrating sensors in this ID chip, the application range can become immense, replacing existing immunoassay devices.

After wafer-level CNT coating, antibodies are coated in a variety of methods including dipping, pipetting, and spotting, etc. Subsequently, the sensor chips are preserved in a storage solution. For medical applications, these chips are soaked in the medical extracts in a small container such as an e-tube and the measurement is performed using a pen type reader by placing the chips on an electrically contactable metal plate biased with constant voltages. Although we use network type CNT sensors, variability issues in the CNT sensors still remain from various reasons, such as non-uniform CNT thickness, metallic CNTs, CNT bundles, etc. To overcome these issues, we used array type CNT sensor where the variability reduces as the size of array increases by the ensemble average effect. For single element immunoassay, we used 32×32 sensor array with antibodies coated all over the chip area. About 50% of sensors (about 500 sensors) with reasonable resistance range are selected, and the diagnosis is made by examining the resistance shift characteristics through a statistical analysis. The larger 64×64 biosensor chip is used for multiplexed testing with multiple spotted antibodies. In this case, the resistance of CNTs in the spotted region increases by liquid effect and this transient resistance change can be measured to locate the valid sensor electrodes for multiple different antibodies [3]. For an actual hepatic cancer detection using a 32×32 sensor array, the first and second color maps show the distribution of CNT resistances after Alpha-fetoprotein antibody immobilization and the application of patient's serum, respectively. As shown in the statistical analysis plot of Fig. 3, we realized a CNT-based immunosensor with reasonable sensitivity for one patient's serum sample. However, the complex nature of biological samples involve many noise components, such as the nonspecific binding, the effect of varying viscosity, and temperature of the samples during sensing, etc. To achieve more reliable diagnosis, the noise components should be reduced by exploring robust immunoassay methods [13] and sensitivity enhancement techniques for electrically measurable biosensors [14].

To explain the efficiency, both in terms of its design simplicity of implementation due to backside rectification and its cost effectiveness due to bare-die measurements, the rest of the paper is organized as follows. Section II describes the benefits of utilizing the backside rectification scheme for the two terminal interface. Section III describes how the sensors in the padless sensor chip are accessed and Section IV discusses the circuitry involved in single I/O line access. Section V demonstrates how the chip can be measured for face up (non-flipped) condition as compared to face down condition (flipped) which we describe throughout the paper. This is followed by a conclusion in Section VI.

II. Backside Rectification

Fig. 4(a) shows the backside rectification scheme using p-substrate to Deep N-well (DNW) PN junction. Through the PN junction, the backside signal voltage can be transferred to the chip VDD node (DNW and N-well) in the $(+)$ voltage condition, while in the $(-)$ voltage condition, the PN junction cuts the connection. With the on-chip capacitance between VDD to VSS (front side metal), the rectified voltage is stabilized to be used as a DC power voltage, while the data signal, which can

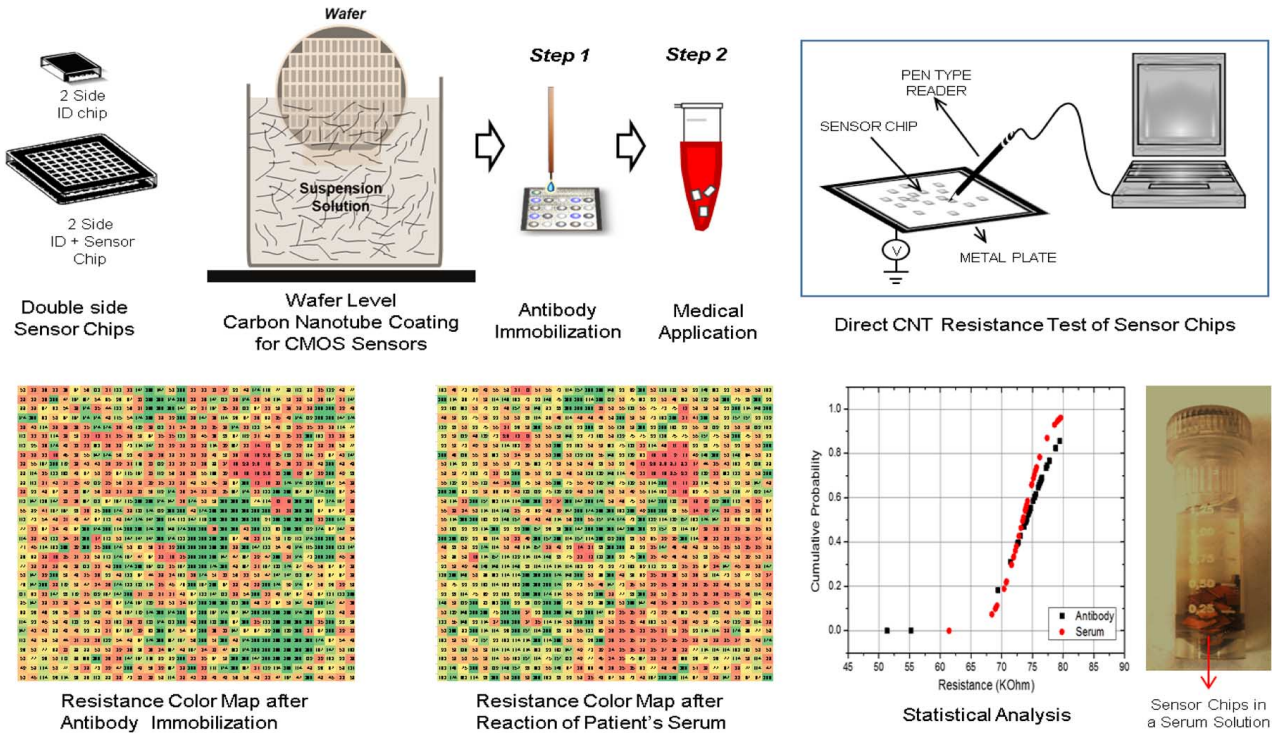


Fig. 3. Overview of sensor preparation and medical application procedures.

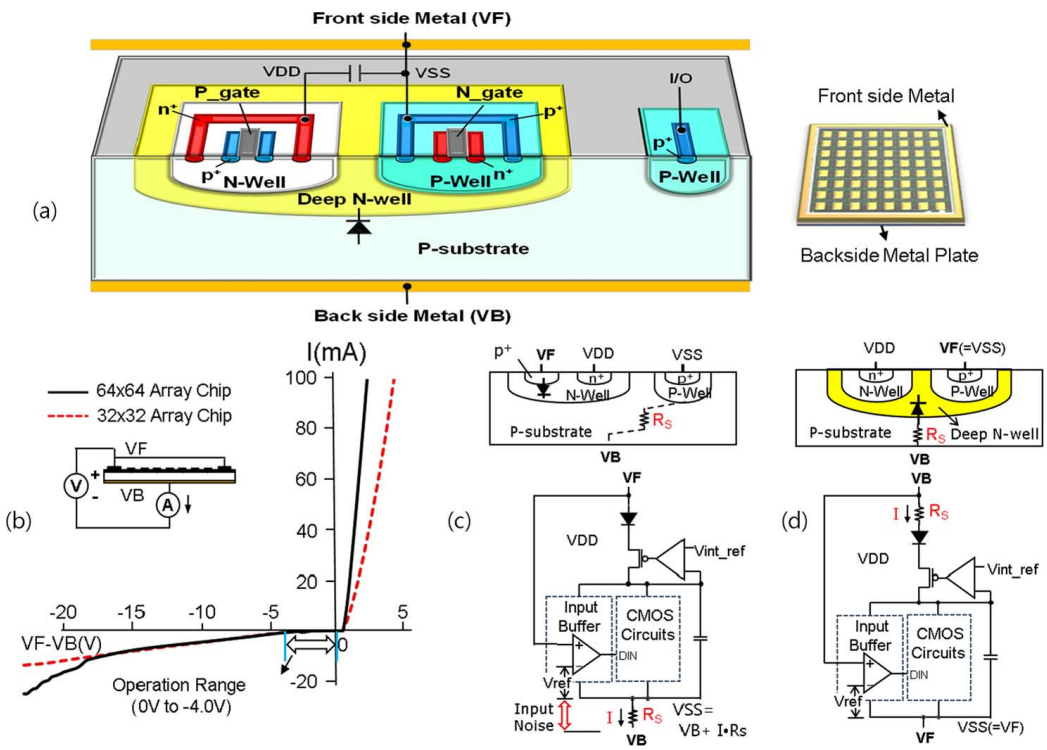


Fig. 4. Simplified structure of backside rectification and advantages over conventional front-side rectification. (a) Backside rectification structure using p-substrate to deep N-well PN junction. (b) Latch-up immunity test result. (c), (d) Ground bouncing noise comparison.

be connected to front side through p-substrate, is used as I/O signal without pad openings.

A. Latchup Immunity

Compared with a conventional PN junction structure, an advantage of this structure is the latch-up immunity. This is because the reverse p-n-p transistor structure has poor transistor current gain due to the poor emitter efficiency and small emitter-

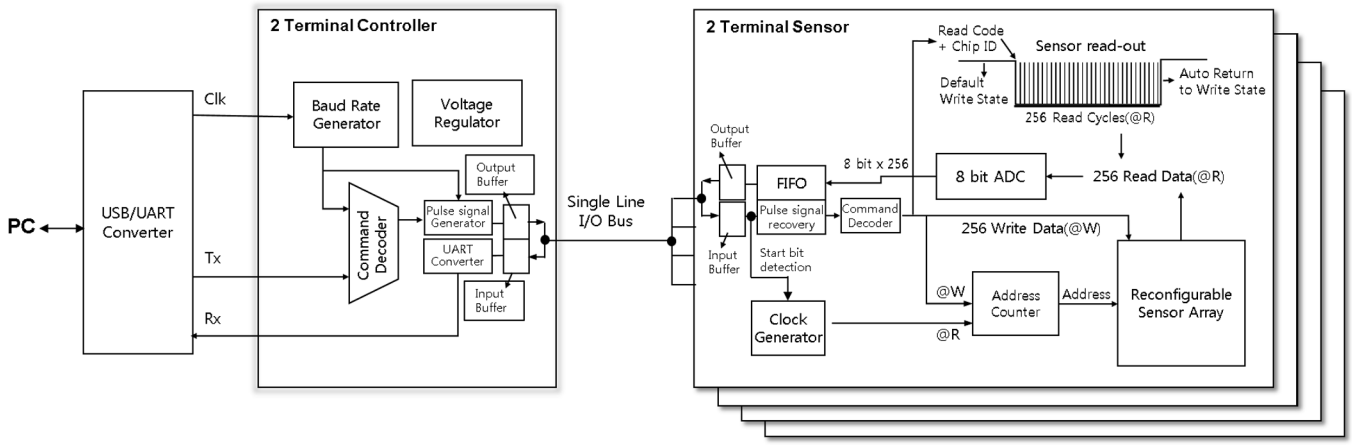


Fig. 5. System block diagram of 2-terminal chip operation.

collector area ratio [15]. Fig. 4(b) shows the latch-up immunity test results for the backside rectification indicating no latch-up up to -20 V.

B. Ground Bouncing Noise

Another advantage of the backside structure is the small I/O interface noises. As shown in Fig. 4(c), conventional structure has ground bouncing problem because the substrate resistance (Rs) is connected in the VSS node. For example, the ground bouncing noise can be as high as 1 V when 20 Ω Rs and an operating current of 50 mA are assumed. For the backside system [Fig. 4(d)], however, Rs is connected in the VDD node, and with a voltage down converter from VDD to Vint, the Vint-VSS power system is stable even under highly loaded conditions.

III. System Block Diagram and Sensor Operation Procedure

Fig. 5 shows the system block diagram and sensor operation flow of 2-terminal chip controller and 2-terminal sensor chips. The 2-terminal controller receives the user command and transmits the received data from the 2-terminal sensors to the external PC via USB/universal asynchronous receiver/transmitter (UART) converter. The system clock running at multiples (x8 or x16) of baud rate frequency of UART communication is used to generate the controller's internal clock to capture the external Tx signal. The internal clock is also used to generate the internal signals for command decoding and pulsed I/O controls. In addition, the internal clock generates the baud rate, which is used for the single line communication to the 2-terminal chips. For Rx output, the received data from 2-terminal chip is logically processed using the internal clock and start and stop bit for UART communication are added to the 8 bit sensed data. For 2- terminal chip operation, the input buffer receives the pulsed I/O line signals and these pulse signals are recovered to the original signal by a toggle flip flop and serially captured by the internally generated constant frequency clock to interpret the meaning of the signals. In the case of arrayed sensor or memory operation, the mode selection of write and read should be performed without external input line signal. For the write mode, which is pre-selected at the chip initialized state, the captured data at the input buffer are decoded in byte size, and delivered to the memory cells of sensors for configuration of the measurement units. A measurement unit consists of 16 sensor selection switches and 8 voltage selection switches where the location in the array is determined by the address counter which increments at every byte input of serial data.

The read mode is selected when the decoded byte signal corresponds to the read mode code. Because this read mode code is commonly detected in the controller and the sensor chip, both chips generate the same number of read clock signals to communicate using 1-line handshaking operation. In addition, if there are multiple sensor chips connected to the I/O line, the read code contains sensor identification code as well to specify a sensor to communicate with. The read clocks in the 2-terminal sensor chip are used to locate the measurement unit serially and to operate the SAR (Successive Approximation Register) type analog to digital converter. For pulsed output of the sensor chip, the FIFO(First-In First-Out) memory which receives the A/D converter results provides the data at the proper timing window of tri-state I/O control and output buffer drives the I/O line according to the FIFO memory output during the switching window. The sense and I/O operations occur in interleaved fashion to protect the sensed analog data from I/O switching noise and to reduce the FIFO memory size. When the predetermined cycles of sensor operation (64 cycles for 32×32 chip and 256 cycles for 64×64 chip) are completed, the read mode is terminated and automatically converted to default write mode to receive another command inputs.

Fig. 6 shows the padless sensor chip layout diagram of 64×64 sensor electrodes. The input and output circuits are connected to the backside, and when read/write(R/W) signal is detected after input decoding, this activates the internal counter to provide serial addresses to the 256 measurement unit decoder which selects the input and output data switches of the measurement units according to the R/W signal states. The internal voltage regulator at the bottom side of the chip generates the regulated voltage for internal chip operation.

Fig. 7(a) shows the sensor electrode structure for the electrical sensor array. The 16 electrodes in the array which share the same area of 1 operational amplifier and 16 programmable switches are grouped to form a measurement unit where the array size of measurement unit is determined by the layout size ratio between

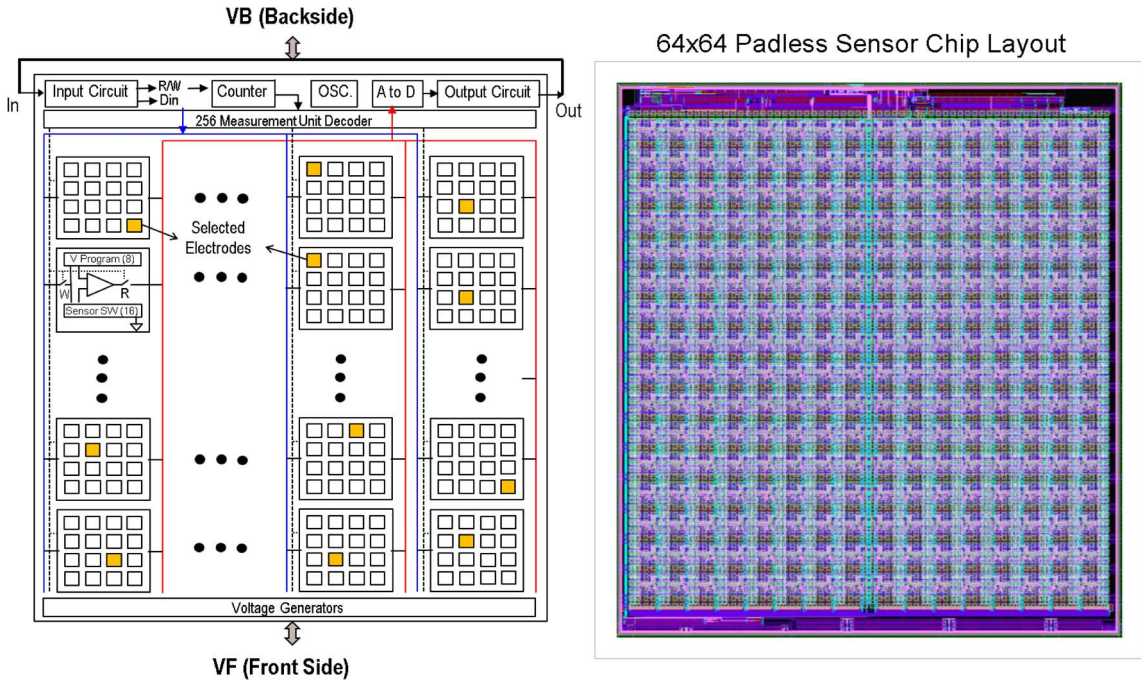


Fig. 6. Chip architecture and layout of 64 × 64 padless sensor chip.

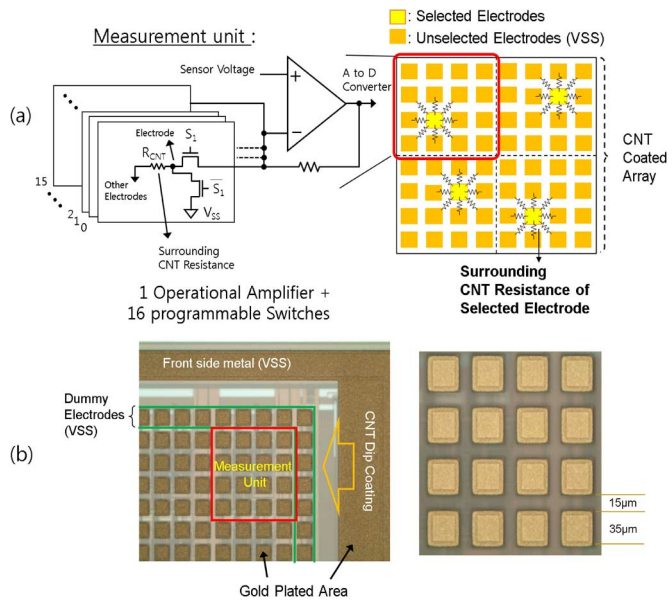


Fig. 7. Sensor electrode structure and surrounding CNT resistance formation. (a) Measurement unit structure. (b) Photographs of gold plated sensor electrodes.

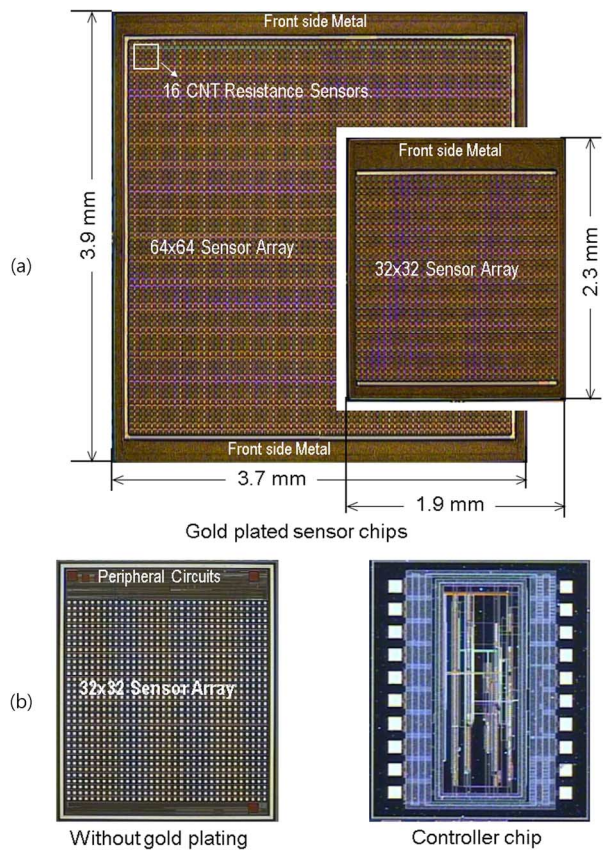


Fig. 8. Photographs of sensor chips and controller chip. (a) Micrographs of the 32 × 32 sensor array chip, and 64 × 64 sensor array chip after gold plating. (b) Micrographs of 32 × 32 chip without gold plating and the controller chip.

the sensor circuitry and the unit electrode. In this unit, when 1 of 16 electrodes is selected by a data input signal, the remaining 15 electrodes are automatically connected to VSS, forming a surrounding CNT resistance sensor. Because only 1 electrode in a measurement unit is connected to the operational amplifier for a data input, to measure all the electrodes in the array, 16 read operations with different data inputs are necessary. The size of each sensor electrode is $35 \times 35\ \mu\text{m}^2$ with 15 μm space between electrodes where this electrode size is determined to achieve optimum sensor performance assuming the average CNT length of 5 μm and 10% metallic CNT composition. Fig. 7(b) shows the photographs of gold plated sensor electrodes. Since the front

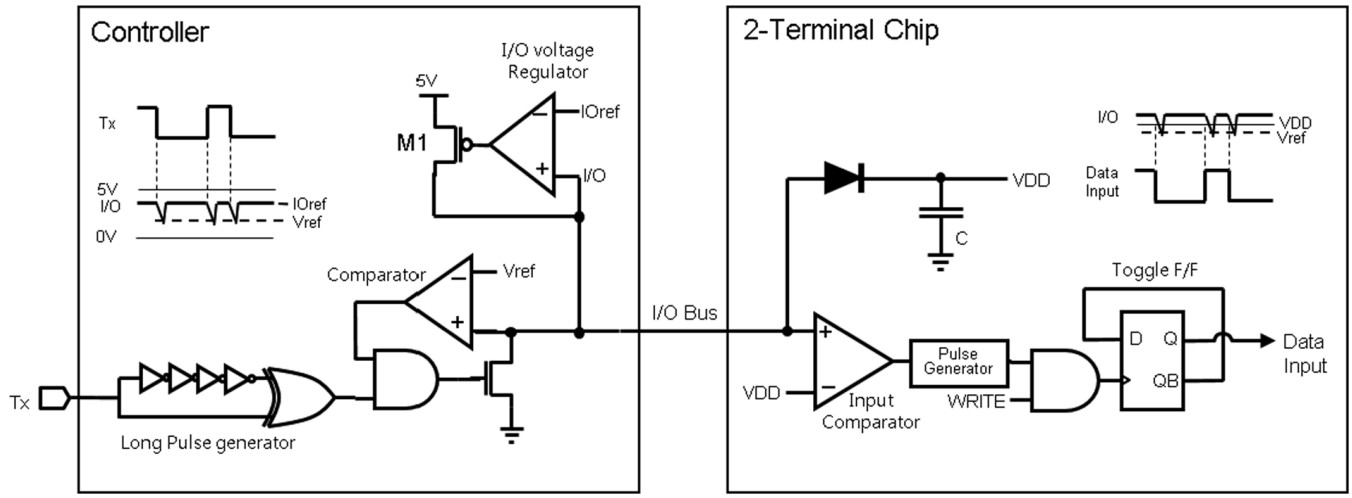


Fig. 9. Data write control circuit.

side metal around the chip and dummy electrodes around the sensor area are at the same VSS potential as the unselected electrodes, wafer-level CNT dip coating is possible because all the CNT areas can have the same potential. This allows obviating the cost incurred for selective CNT coating [6].

Fig. 8(a) shows the die micrographs of the 32×32 and 64×64 sensor array chips after gold plating process. There are no pads on these chips and occupy areas of $1.9 \times 2.3\ \mathrm{mm}^2$ and $3.7 \times 3.9\ \mathrm{mm}^2$, respectively. Fig. 8(b) shows the same 32×32 chip without gold plating and the controller chip which is used to operate the padless sensors. The controller chip occupies the same area as the 32×32 sensor array chip.

IV. Circuit Implementation

An existing 1-wire communication protocol uses open drain style data I/O with pull-up resistor and pulse-width-modulation (PWM) style data recognition system [16]. However, to enable stable sensing of multiple resistors in an array, a new pulse based communication scheme has been developed. The main idea of this scheme is reducing the power degradation during the data signaling time. In the case of flipped orientation, data signaling is initiated using "low" signals, and the power dissipation during that time must be minimized because the sensor chip is supplied by the rectified power of "high" signals. Fig. 9 shows the data write control circuit, which covers the Tx path from controller to sensors. The controller on the left and the padless sensor chip on the right are connected through single I/O line. For this communication system, the sensor chip power is supplied by the rectified voltage of I/O line. The I/O voltage regulator sets the I/O reference voltage level and short Vref limited pulses are made at Tx transitions. These pulse signals are transferred through the single I/O line to the sensor chip. The input buffer detects the presence of pulse by comparing the I/O level with the internal reference voltage (VDD in this case) and generates a pulse, which is used for the toggle flip-flop to recover the original Tx signals.

A concern of diode rectification and pulsed I/O scheme for single line communication is the VDD droop by I/O signal coupling. Fig. 10 shows the droop generation mechanism. When Tx transition occurs, I/O pulse of limited size is generated and the VDD drooping by I/O signal coupling is observed. To reduce the VDD drooping, large reservoir capacitance of VDD is needed.

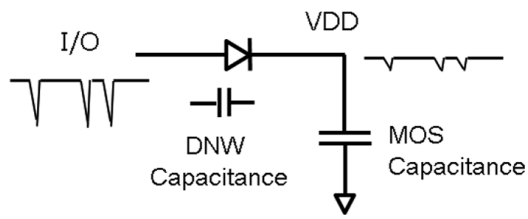


Fig. 10. VDD droop mechanism due to I/O signal coupling.

The size of VDD drooping is described in (1)

$$Vdroop = \frac{\mathrm{C1} * \mathrm{Vpulse}}{\mathrm{C1} + \mathrm{C2}} \tag{1}$$

Where C1 is diode capacitance formed between the p-substrate and Deep N-well region, and C2 is the reservoir MOS capacitance made using very thin gate oxide layer. MOS capacitor is the VDD reservoir capacitance which is formed under the routing area, and assumed to have 1/4 of the Deep N-well area. Even though Deep Nwell area is larger than MOS capacitance area, the DNW capacitance is less than 1/20 of MOS capacitance. In this regard, C2 is about $5 * \mathrm{C1}$ and the VDD drooping from the equation is about $0.17 * \mathrm{Vpulse}$ and thus be managed to be less than 1/5 of the VDD using the MOS capacitor.

Fig. 11 shows the data read control circuit which covers the Rx path from sensor to controller. To be able to detect the sensed data preserving the pulsed communication method, we developed a tri-state I/O control by detecting the I/O voltage level. In the controller and sensor circuits, the constant pulse generator (CPG) circuit is commonly placed. When read command is given by read clock (Rclk), the I/O line is pulled down like a write cycle. However, when the I/O line reaches Vref level, CPG circuit generates a pulse which makes the data line float (by turning off the M2) and receives the data outputs from the sensor chip. As shown in the timing diagram, the I/O voltage level changes according to the data output of sensor chip (Data

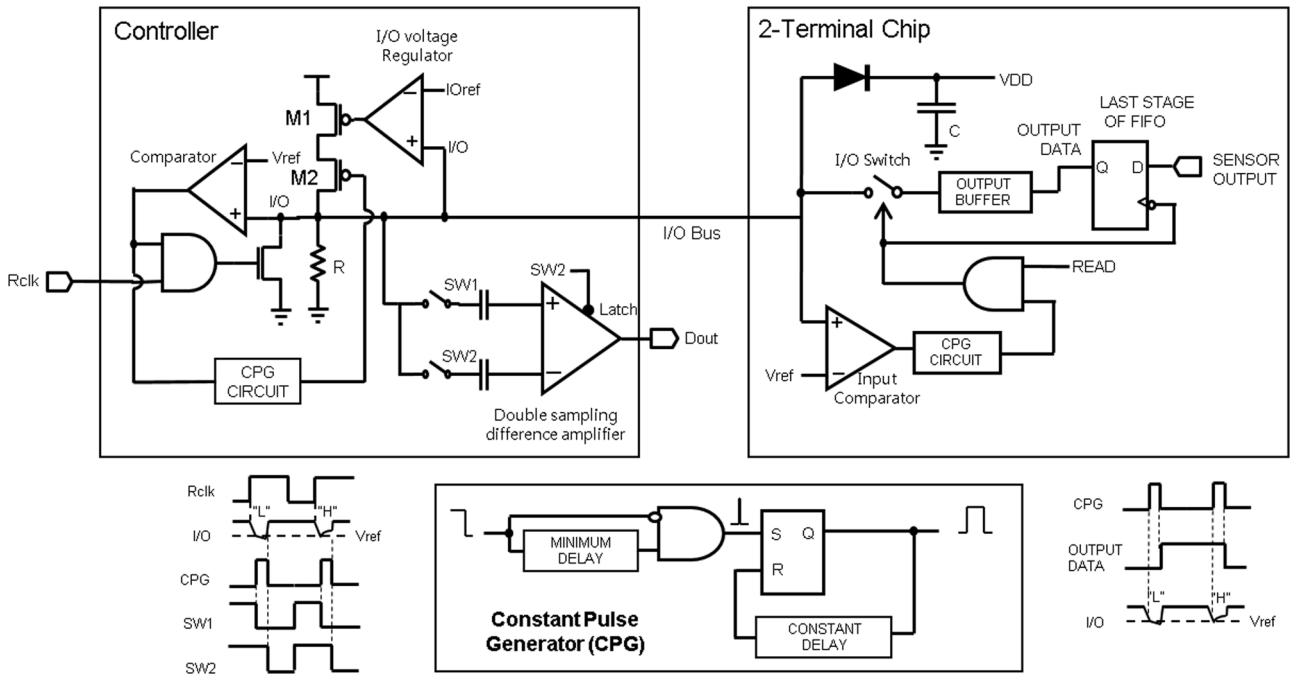


Fig. 11. Data read control circuit with level sensitive switch control.

"L" or Data "H" in the figure). The received data are sensed by a double-sampling difference amplifier (sampled by SW1 and SW2 signals) and latched when the CPG signal returns. The I/O line voltage is regulated to the voltage IOref by M1, and the external pull-down resistor R is used to calibrate the read data level against the sensor system variation.

Read operation of 2-terminal sensor chip is closely related to the controller operation for the tri-state I/O interface. Under the data read mode, when input buffer detects the I/O signal level (Vref) from the controller, the I/O switch turns on to send the sensor data to the I/O line. Since the controller detects the same I/O signal level (Vref) in the common I/O line connection, the data read window is self-synchronized between controller and sensor chip as long as the CPG pulse width of both chips are controlled to be the same. This enables a very short data recognition time, which leads to small power fluctuation and high data rate communication.

Fig. 12 shows the timing diagram of main signals in the UART communication using 1 line pulsed I/O scheme.

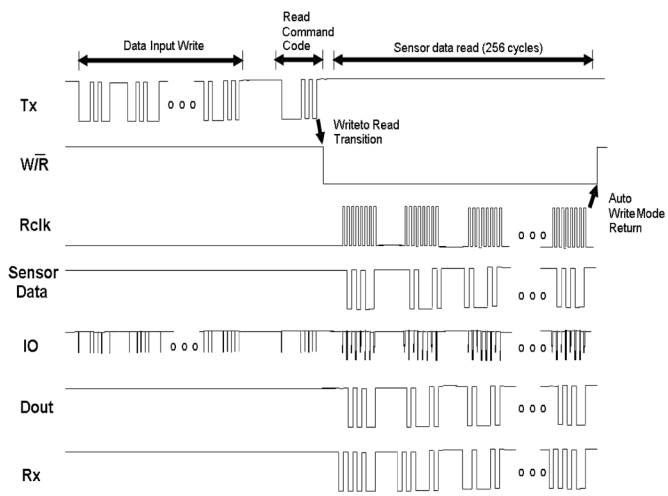


Fig. 12. Timing diagrams of UART communication using 1 line pulsed I/O scheme.

V. Circuit for Flippable Bare-Die Probing

A special issue that arises for bare die probing is that the chip could be either flipped or nonflipped depending on measurement procedures. It is natural that reversed I/O biasing from controller with exchanged sensor terminals gives identical sensor operation in the 2-terminal system.

Fig. 13(a) shows the control circuits with reversed I/O voltage control. Compared with the controller part of the Fig. 11, this circuit generates the reverse polarity I/O signals that have rising pulses of the same size as the falling pulses of Fig. 11. From the 2-terminal device biasing theory, if we connect this I/O signal to the VF terminal (instead of VB terminal) with VB terminal of constant VCC potential (instead of pulsed I/O voltage), the sensor operation is identical to the previous operation. Fig. 13(b) is the circuit to realize both cases using mode selection switches. In this circuit, mode selection switches (mode1 for flipped, and mode2 for non-flipped) are added and exclusively controlled without data contention issues. I/O voltage levels are controlled to IOref1 (mode1 I/O voltage) and IOref2 (mode2 I/O voltage) by voltage regulators VG1 and VG2, respectively. As shown in the connection diagram (Fig. 13(c)), for mode1 case, I/O line is connected to the VB terminal with common VF terminal. The VF level is ground, and I/O signal is represented by falling pulses. While for mode2 case, I/O line is connected to the VF terminal with common VB terminal. The VB level is VCC, and I/O signal is represented by rising pulses.

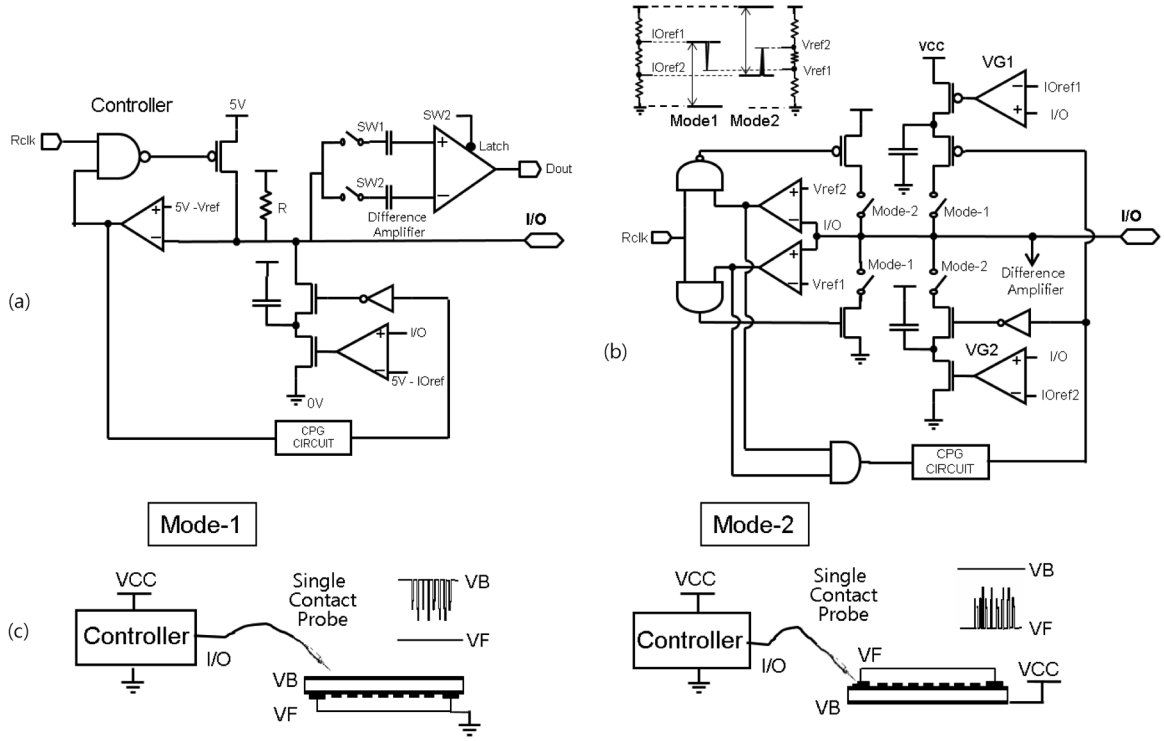


Fig. 13. Control circuits and connection diagrams of flippable bare-die probing method. (a) Control circuits with reversed I/O voltage control. (b) Control circuits for flippable bare-die probing by mode selection. (c) Connection diagrams of flippable probing method for mode-1 and mode-2.

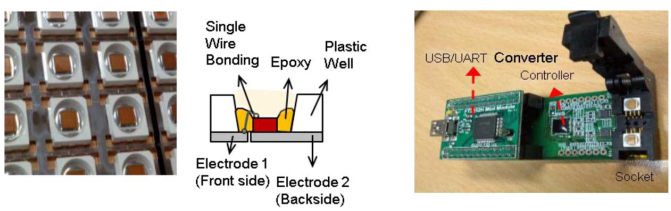


Fig. 14. System packaging and test board for measurement.

VI. Measurement Results

For measurement of padless sensors, chip is thinned down to 300 μm to reduce substrate resistance, and reliable backside metallization is performed. Because the bare-die measurement can be dependent on the contact resistances between metal plate and chip as well as pen type reader and the chip, we made a temporary package for stable measurement. Because there are only 2 terminals, we could use the existing LED lead frame for packaging. Fig. 14 shows the temporary package and the test board where 2 different test chips can be tested using 1 common controller. For medical applications using these packaged samples, a chip with known characteristics is used as a calibration reference and the other chip is used for actual measurement to reduce the statistical average drift effect. The tested results can be sent to the PC through a conventional USB/UART converter module such that they can be analyzed using PC programs.

Fig. 15 shows the measurement results. For mode1 and mode2 write operations, I/O pulse signals are generated right after the UART Tx signal transitions. The insets show the swing voltage is about 2.2 V at 4.0 V I/O voltage and the write pulse width is about 0.1 μsec. For mode1 and mode2 read operations, I/O pulse signals show different depths depending on the "high" and "low" data from the sensor chip and corresponding Rx signals are generated. The insets show the "high" and "low" level differences at signal latching time are about 0.7 V and the read pulse width is about 0.2 μsec. From these measurement results, the estimated maximum data rate is 2 MHz with 0.3 μsec I/O line restore time.

Fig. 16 shows the resistance color map of 32 $\times$ 32 sensor chips.

To check the repeatability, we performed 4-times repeated CNT resistance measurements. These resistance map can be used for medical applications if we apply these tests in the different stages of sample preparation, and extract the statistical meanings through an analysis software.

Table I summarizes the performance of double side CMOS-CNT biosensor chip.

VII. Conclusion

We proposed a disposable biosensor chip to facilitate simple and cost effective medical tests. This chip can take advantage of backside rectifying diode with a high latch-up resistance and low ground bounce noise. Using this technology, bare die measurement without microfluidic channel is possible. Furthermore, nano-material typically required for high sensitivity sensors is coated in wafer-level instead of costly selective coating. The measured results show higher data rate than current 1-wire communication protocols and stable operation under high loaded conditions. As a result, a stable operation under 150 mW maximum power at 2 MHz data rate can be achieved.

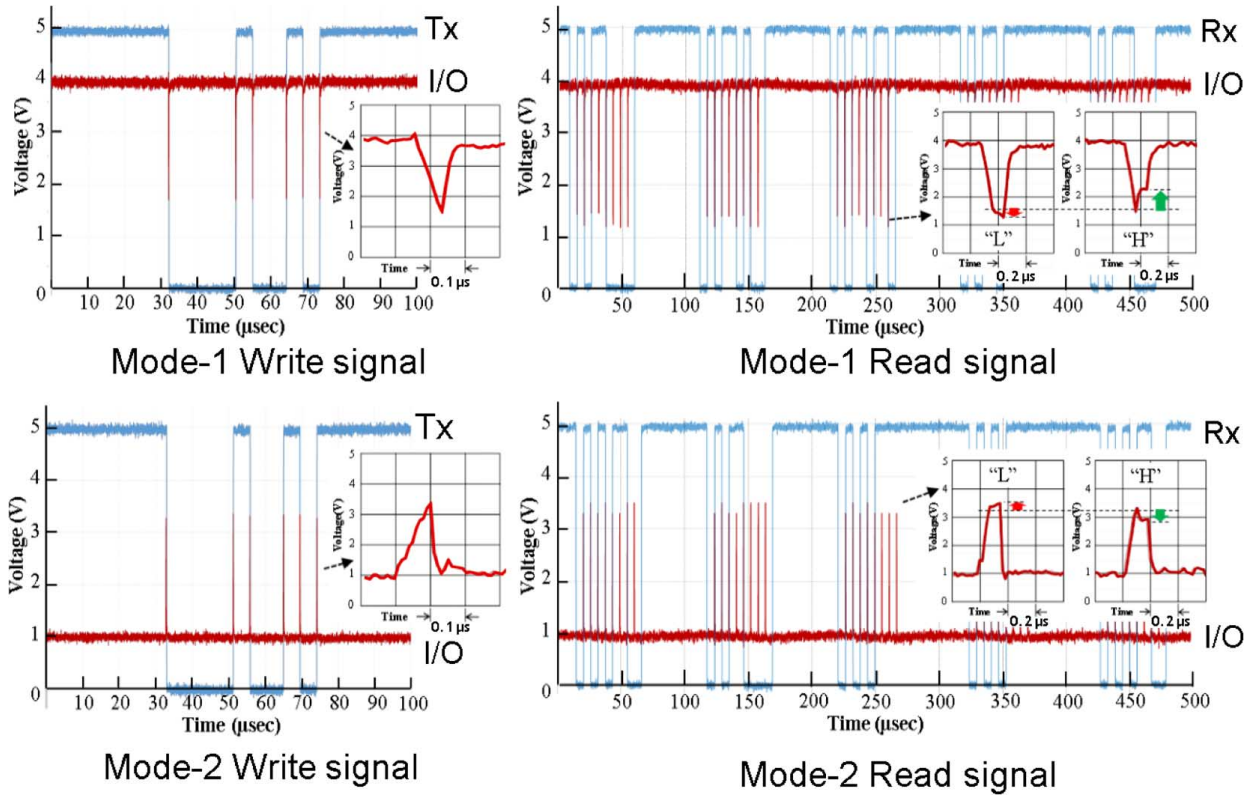


Fig. 15. Measurement results for mode-1 and mode-2 chip operations.

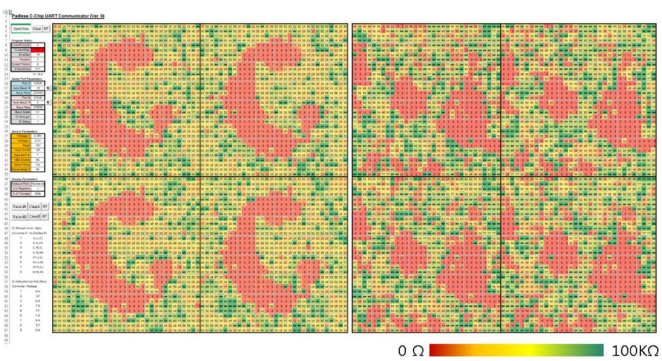


Fig. 16. Resistance color map of 2 padless chips by 4-times repeated testing.

TABLE I
PERFORMANCE SUMMARY OF SENSOR CHIP

Process Technology	0.35μm CMOS process(Magnachip)
Controller Voltage, I/O line Voltage	5.0V 4.0V
Sensor Chip Voltage	3.3 V, 2.5V(internal)
Maximum Data Rate	2.0 Mbps
Resistance Range	5KΩ(min.), 100KΩ(max.)
ADC	2.5V, 8 bit SAR
Latch-up Voltage	> 20V
Power Consumption	5 mW(min.), 150 mW(max.) → depending on CNT resistance
Chip Area	1.9 x 2.3 mm^2 (1K Sensor) 3.7 x 3.9 mm^2 (4K Sensor) 1.9 x 2.3 mm^2 (Controller)

ACKNOWLEDGMENT

The authors thank MagnaChip Semiconductor for chip fabrication.

REFERENCES

[1] J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai, "Nanotube molecular wires as chemical sensors," *Science*, vol. 287, pp. 622–625, 2000.

[2] K. Besteman, J. Lee, F. G. M. Wiertz, H. A. Heering, and C. Dekker, "Enzyme-coated carbon nanotubes as single-molecule biosensors," *Nano Lett.*, vol. 3, no. 6, pp. 727–730, 2003.

[3] J. W. Ko, J. M. Woo, J. Ahn, J. H. Cheon, J. H. Lim, S. H. Kim, H. Chun, E. Kim, and Y. J. Park, "Multi-order dynamic range DNA sensor using a gold decorated SWCNT random network," *ACS Nano*, vol. 5, no. 6, pp. 4365–4372, 2011.

[4] J. Ahn, S. H. Kim, J. Lim, J. W. Ko, C. H. Park, and Y. J. Park, "Analysis of sensing mechanisms in a gold-decorated SWNT network DNA biosensor," *J. Semicond. Technol. Sci.*, vol. 14, no. 2, pp. 153–162, 2014.

[5] E. Y. Jang, T. J. Kang, H. W. Im, D. W. Kim, and Y. H. Kim, "Single-walled carbon-nanotube networks on large-area glass substrate by the dip-coating method," *Small*, vol. 4, no. 12, pp. 2255–2261, 2008.

[6] Q. Fu, C. Lu, and J. Liu, "Selective coating of single wall carbon nanotubes with thin SiO_2 layer," *Nano Lett.*, vol. 2, no. 4, pp. 329–332, 2002.

[7] P. Qi, O. Vermesh, M. Grecu, A. Javey, Q. Wang, H. Dai, S. Peng, and K. Cho, "Toward large arrays of multiplex functionalized carbon nanotube sensors for highly sensitive and selective molecular detection," *Nano Lett.*, vol. 3, no. 3, pp. 347–351, 2003.

[8] S. Khamis, R. Jones, and A. C. Johnson, "Optimized photolithographic fabrication process for carbon nanotube devices," *AIP Adv.*, vol. 1, p. 022106, 2011.

[9] B. Jang and A. Hassibi, "Biosensor systems in standard CMOS processes: Fact or fiction?," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 979–985, 2007.

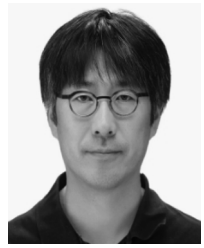
[10] M. Usami, H. Tanabe, A. Sato, I. Sakama, Y. Maki, T. Iwamatsu, T. Ipposhi, and Y. Inoue, "A 0.05 × 0.05 mm2 RFID chip with easily scaled-down ID-memory," in *Proc. ISSCC Dig. Tech. Papers*, 2007, pp. 482–483.

[11] O. Beske, J. Guo, J. Li, D. Bassoni, K. Bland, H. Markiniac, M. Zarowitz, V. Temov, I. Ravkin, and S. Goldbard, "A novel encoded particle technology that enables simultaneous interrogation of multiple cell types," *J. Biomol. Screen.*, vol. 9, pp. 173–185, 2004.

[12] W. Mandecki, B. Ardelt, T. Coradetti, H. Davidowitz, J. A. Flint, Z. Huang, W. M. Kopacka, X. Lin, Z. Wang, and Z. Darzynkiewicz, "Microtransponders, the miniature RFID electronic chips, as platforms for cell growth in cytotoxicity assays," *Cytometry A*, vol. 69, no. 11, pp. 1097–1105, 2006.
[13] S. MacKay, D. Wishart, J. Xing, and J. Chen, "Developing trends in aptamer-based biosensor devices and their applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 4–14, Feb. 2014.
[14] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise limits of CMOS current interfaces for biosensors: A review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 278–292, Apr. 2014.
[15] S. M. Sze*, Semiconductor Devices: Physics and Technology*, 2nd ed. New York, NY, USA: Wiley, 1985, pp. 140–147.
[16] Maxim Integrated [Online]. Available: http://pdfserv.maximintegrated.com/en/an/AN74.pdf(25-05-2013)

Jinhong Ahn received the B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively.

From 1984–1999, he was with LG Semiconductor as a Memory Design Engineer. From 1999–2008, he was with Hynix Semiconductor as a Research Fellow of advanced DRAM design. Since 2008, he has been with Nano Systems Institute (NSI) at Seoul National University as a Principal Researcher. Currently, he is the President of Duality Inc., Daejeon, Korea. His research areas at NSI were electrical sensors using nano materials and array type biosensor chip design for medical applications.



Sang Hoon Hong received the B.S. degree from Yonsei University, Seoul, Korea, and the M.S. and Ph.D. degrees from Harvard University, Cambridge, MA, USA, all in electrical engineering.

Currently, he is an Associate Professor in the Department of Electronics and Radio Engineering at Kyung Hee University, Yongin, Korea. His research interest focuses on parallel processing circuits, the application of which includes hardware search engines, image sensors for augmented reality, and 3D graphics hardware.

Youngjune Park (M'77) received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, and the Ph.D. degree from the University of Massachusetts, Amherst, MA, USA, in 1975, 1977, and 1983, respectively, all in electrical engineering.

From 1983–1988, he worked for IBM, East Fishkill, NY, USA, and LG Semiconductor, Seoul, as a research staff member. In 1988, he joined Seoul National University as a faculty member and has contributed to education, semiconductor lab establishment, consulting to companies (as the R&D Director at SK Hynix) and the government of Korea. His research areas of interest include the nano semiconductor device physics, reliability, and bio molecular sensing using semiconductor devices.