Towards High Throughput Cell Growth Screening: A New CMOS 8 × 8 Biosensor Array for Life Science Applications

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***Abstract*—In this paper we present a CMOS capacitive sensor array as a compact and low-cost platform for high-throughput cell growth monitoring. The proposed biosensor, consists of an array of 8 × 8 CMOS fully differential charge-based capacitive measurement sensors. A DC-input ΣΔ modulator is used to convert the sensors' signals to digital values for reading out the biological/chemical data and further signal processing. To compensate the mismatch variations between the current mirror transistors, a calibration circuitry is proposed which removes the output voltage offset with less than 8.2% error. We validate the chip functionality using various organic solvents with different dielectric constants. Moreover, we show the response of the chip to different concentrations of Polystyrene beads that have the same electrical properties as the living cells. The experimental results show that the chip allows the detection of a wide range of Polystyrene beads concentrations from as low as 10 beads/ml to 100 k beads/ml. In addition, we present the experimental results from H1299 (human lung carcinoma) cell line where we show that the chip successfully allows the detection of cell attachment and growth over capacitive electrodes in a 30 h measurement time and the results are in consistency with the standard cell-based assays. The capability of proposed device for label-free and real-time detection of cell growth with very high sensitivity opens up the important opportunity for utilizing the device in rapid screening of living cells.**

***Index Terms*—Capacitive sensor array, cell growth monitoring, CMOS, high-throughput screening.**

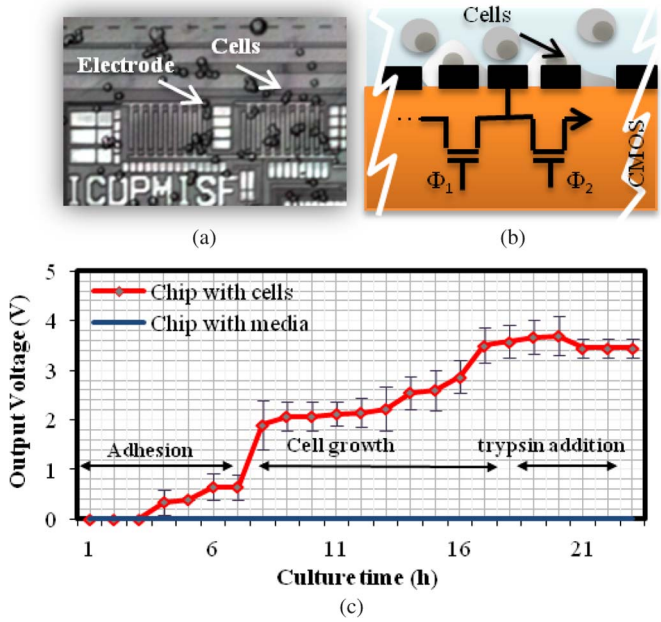

Fig. 1. Illustration of recently proposed capacitive sensor for cellular analysis. (a) Cells attached on the interdigitated electrodes. (b) Simple illustration of CBCM circuitry. (c) Response of the chip to adherent H1299 cells.

I. Introduction

CMOS capacitive sensors have recently attracted the attentions for a variety of life science applications such as genetic analysis, infectious disease detection, and cellular studies [1]–[3]. A capacitive sensor consists of an interface circuit connected to capacitive electrodes realized in the top most metal layer in CMOS process. Among various interface circuit topologies, charge based capacitive measurement (CBCM) technique has demonstrated great advantages as highly accurate technique for sensing applications [4], [5]. CBCM was initially proposed for the measurement of cross talk capacitance in between the conductors in CMOS chips using off-chip DC ammeter [6]. Ghafar-Zadeh *et al.* took this technique to another level by developing an integrated single-ended ΣΔ charge to digital converter for Lab-on-Chip applications [7]. In another effort, Nabovati *et al.* reported a fully differential core-CBCM interface circuit for chemical solvent monitoring [8]. As a follow-up to that work, we used the same chip for cellular growth monitoring [see Fig. 1(a) and (b)]. This figure shows the attachment of H1299 cells on the surface of CMOS chip. Following a standard cell culture procedure, the cells were prepared and introduced to the CMOS sensor. All tests were performed in triplicates to demonstrate the chips functionality. As seen in Fig. 1(c), the sensor can detect two phases of adhesion and growth in the cell culture followed by trypsinization process which leads to cell detachment from the

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sensing electrodes. These promising results, shown in Fig. 1, have inspired the idea of developing an array of large number of capacitive micro-sensors integrated on the same chip for high-throughput screening. In this paper, we take the first step toward this goal by developing an array of 8×8 interdigitated electrodes interconnected to fully differential $\Sigma\Delta$ charge to digital converters.

High-throughput cell culture screening is the key challenge for a variety of life science applications including drug discovery and cytotoxicity monitoring [9], [10]. To date, several efforts have been made to develop microfluidic devices featuring arrays of micro-chambers for cell culture screening using optical microscopic techniques [11], [12]. However less attention have been paid on developing integrated sensors incorporated with cell culture micro-wells for monitoring cellular activities such as tumor cell proliferation and cytotoxicity monitoring using capacitive or Ion-Sensitive Field Effect Transistors (ISFETs) [13], [14]. Among these, capacitive techniques by offering low complexity platform have significantly attracted attentions as a mean to study cell-surface interaction that can be important for a variety of biological studies [15], [16]. Despite these great advances, still the development of a large number of capacitive micro-sensors for high-throughput screening is a challenge. These challenges can appear both in circuit design level or integration level. In circuit design process, due to the large array of sensing electrodes, the effect of parasitic and cross talk could be considerable, hence choosing the right electrode structure and dimension is very important. It is proved that choosing the electrode features close to the test analytes, can optimize the sensor performance. However, in cell-based applications, due to the small capacitance of the sensor, the detection sensitivity are limited by noise resulted from large parasitic capacitance that is many orders of magnitude greater than the sensor capacitance. Besides, the electronic noise from the readout circuit also affects the measured accuracy. Therefore, they should be considered for the development of sensitive and accurate sensing devices. On the other hand, the inclusion of CMOS technology in the applications that necessitates the direct contact of sensing or actuation electrodes with the chemical/biological solutions complicates the packaging and encapsulation process. The packages not only should protect the device from the solutions but also it should be robust enough against several cleaning procedures and long-term experiments such as cell culture monitoring that can last up to 1 week. In this paper we address these challenges by developing a CMOS sensor array consisting of 64 capacitive electrodes. In the remainder of this paper we will discuss the design and implementation of this chip in Section II, followed by a discussion on its design optimization in Section III. The results of fabricated chip and biological/chemical experiments will be discussed in Section IV. This section is followed by the conclusion in Section V.

II. Fully Differential Capacitive Sensor Array Design and Implementation

The proposed CMOS cell-based biosensor consists of a capacitive sensor system as shown in Fig. 2(a). In this section, we put forward the details of this system including 64 capacitive sensors (C_S), eight decoders, eight $\Sigma\Delta$ ADCs, and eight reference electrodes along with calibration circuitries. A FPGA system is also used to generate clocks (Φ_1, Φ_2, Φ_3, and Φ_4) in order to activate CBCM structure and DC-input $\Sigma\Delta$ modulators and finally readout the data from capacitive electrodes (C_Ss). Also this FPGA controls the decoder and calibration circuits accordingly.

A. Differential Charge to Voltage Converter

The fully differential charge to voltage converter consists of a CBCM structure ($M_1 - M_4$), integrating capacitors ($C_{\mathrm{int}+}, C_{\mathrm{int}-}$) and several current mirrors as was previously described in [8]. As shown in Fig. 2(b), the sensing current $I_S^{i,j}$ which is charging the capacitive sensing electrodes ($C_S^{i,j}$) is described by

$$I_S^{i,j} = C_S^{i,j}\frac{dV_{\mathrm{SE}}}{dt} = \beta(V_{\mathrm{DD}} - V_{\mathrm{SE}} - V_{\mathrm{thp}})^2 \tag{1}$$

where V_{DD} is a power supply voltage, V_{SE} is the voltage dropped on sensing capacitor, V_{thp} is the pMOS threshold voltage, $V_{\mathrm{DD}} - V_{\mathrm{SE}}$ is M_2 gate-source voltage, $0 < i, j \leq 8$, and β is transistors parameter and is equal to $\mu_n C_{\mathrm{ox}} W/L$ where μ_n is the surface mobility of charge carrier in MOS device, C_{ox} is the gate insulator capacitance and W/L is MOS transistor's aspect ratio.

By solving the above differential equation and by assuming that the sensing and reference electrodes are fully discharged at $t = 0$, then the transient value of voltage on sensing electrode is given by

$$V_{\mathrm{SE}} = \frac{C_S(V_{\mathrm{DD}} - V_{\mathrm{thp}})}{\beta(V_{\mathrm{DD}} - V_{\mathrm{thp}})t + C_S} + V_{\mathrm{DD}} - V_{\mathrm{thp}}. \tag{2}$$

The transient current, that charges the integrating capacitor can be calculated as

$$I_S^{i,j} = \frac{K_1 C_S^{i,j^2}(V_{\mathrm{DD}} - V\mathrm{thp})^2}{\left(\beta(V_{\mathrm{DD}} - V\mathrm{thp})t + C_S^{i,j}\right)^2} - \frac{K_2 K_3 C_R^2(V - \mathrm{DD} - V\mathrm{thp})^2}{\left(\beta(V_{\mathrm{DD}} - V\mathrm{thp})t + C_R^i\right)^2} \tag{3}$$

where K_1, K_2, and K_3 are the first (M_5, M_7), second (M_6, M_8) and third (M_9, M_{10}) current mirrors' amplification factors. The final value of current that is charging the integrating capacitor is calculated by the following equation

$$I_S^{i,j} = f_s\left(K_1 C_S^{i,j} - K_2 K_3 C_R^i\right)(V_{\mathrm{DD}} - V\mathrm{thp}). \tag{4}$$

We assume that in each Φ_2 clock pulse period the capacitances are fully charged to approximately V_{DD} and we also assume that $K_1 = K_2 K_3 = K$. Due to the circuit symmetry, the same equations exist for both currents charging $C_{\mathrm{int}+}$ and $C_{\mathrm{int}-}$ but with a negative sign for the latter. The output voltage is obtained by

$$V_{\mathrm{out}}^{i,j} = \frac{2K\Delta C^{i,j} V_{\mathrm{DD}} f_{\mathrm{int}}}{C_{\mathrm{int}} f_s} = \frac{2K\Delta C^{i,j} V_{\mathrm{DD}} N}{C_{\mathrm{int}}} \tag{5}$$

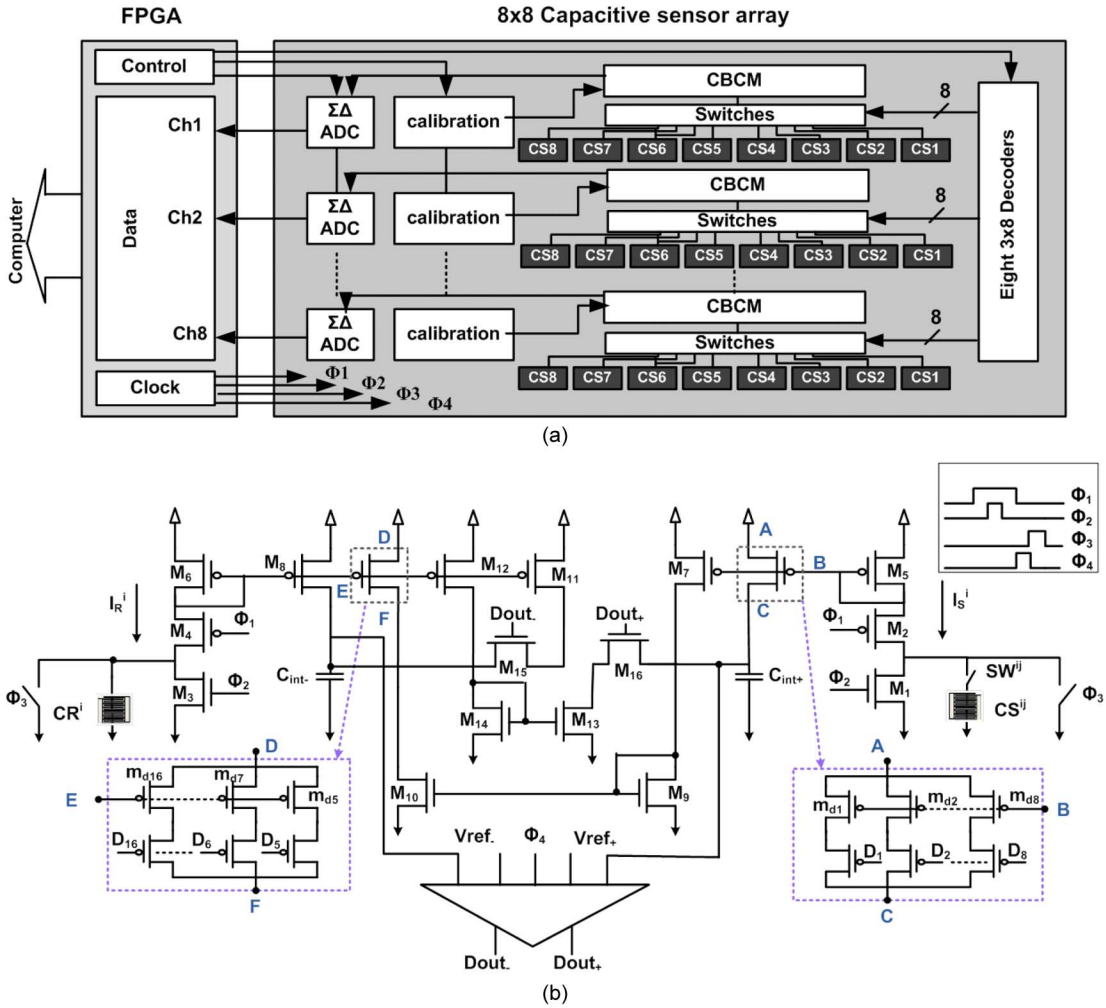

Fig. 2. (a) System level block diagram of proposed cell-based capacitive sensor, CSs blocks refer to interdigitated sensing electrodes, and CBCM refers to charge based capacitive measurement circuit block. (b) Circuit implementation of capacitive readout interface.

where $\Delta C^{i,j} = C_S^{i,j} - C_R^i$ and f_s is the frequency of Φ_2, $C_{\rm int} = C_{\rm int+} = C_{\rm int-}$ is the integrating capacitance, and $f_{\rm int}$ is the frequency of Φ_3. As it is seen from (5), as the number of integration cycles (N) increases, the output gain also increases. In other words, the sensitivity of the circuit can be adjusted by changing the ratio of $f_{\rm int}$ and f_s. We will use this feature to control the sensitivity and dynamic range of the CBCM circuit.

B. DC-Input ΣΔ Modulator

The proposed ΣΔ modulator is realized by adding a voltage comparator, and a digital to analog converter to the described readout structures as shown in Fig. 2(b). Considering the differential architecture, two DACs, one with the negative current (M_{13}) and one with positive current (M_{11}) are added to the core-CBCM interface circuit. To implement the quantizer block, a 4-input comparator is adapted from [17] and modified for use in the CBCM circuit. Eight ΣΔ modulators are implemented in the array and the output bit-stream is collected and decoded using custom-made Labview data-acquisition system through an averaging routine that will be described later.

C. Sensing Electrodes Array

A complete capacitive sensor array is realized by integrating switches $\rm SW^{i,j}$, $0 < i, j \leq 8$ and 3×8 decoders as seen in Fig. 3. The capacitive sensing electrodes, fabricated on topmost metal layer of CMOS chip play the important role of interfacing between readout circuitry and test solution. Each pixel in the array is composed of a pair of interdigitated electrodes which is patterned in M4 metal layer in TSMC 0.35 μm CMOS technology. The dimensions of the electrode are specifically designed to fit the area constraints of CMOS chip and maximising the sensing sensitivity. The interdigitated electrode size is 50×50 μm^2, comprising four fingers with 5 μm spacing. In order to make a direct contact with analyte solutions, the passivation layer in CMOS technology was removed in foundry process using etching techniques and the aluminum layer is used as the sensing layer. During the biological experiments, in order to protect the aluminium from direct exposure to cell culture solutions and also to provide a better electrode biocompatibility, a thick layer of Polydimethylsiloxane (PDMS) is deposited on the electrodes serving as the passivation layer. More details about the PDMS deposition process are provided in Section IV-B.

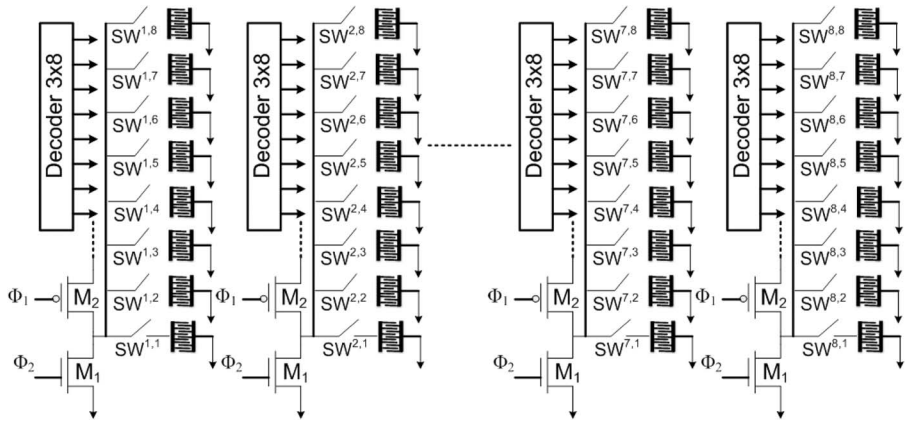

Fig. 3. Capacitive sensor array and corresponding addressing circuit. SW switches are controlled by 3 × 8 decoders and they are connecting the sensing electrodes to core-CBCM circuits.

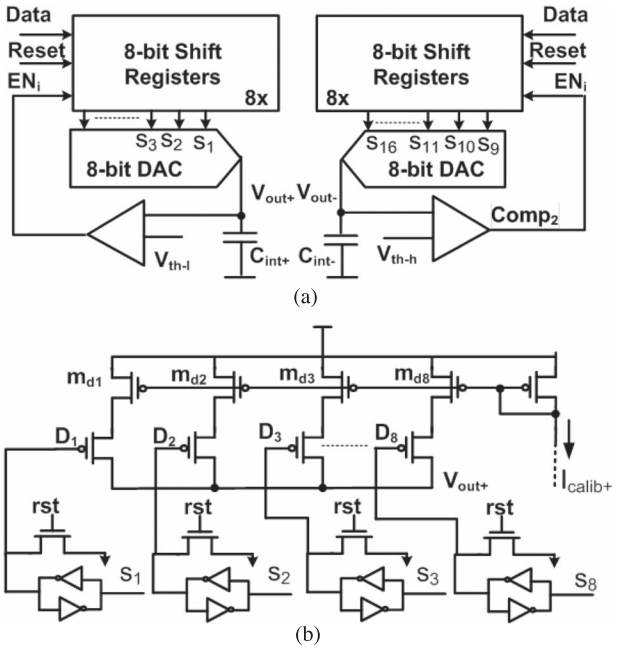

Fig. 4. (a) Simplified block diagram of calibration circuitry. (b) Latched DAC with reset input. In each calibration clock, the output voltage is compared with the reference voltage, based on the difference with the reference voltage, the 4-bit DACs currents charging the integrating capacitors are adjusted.

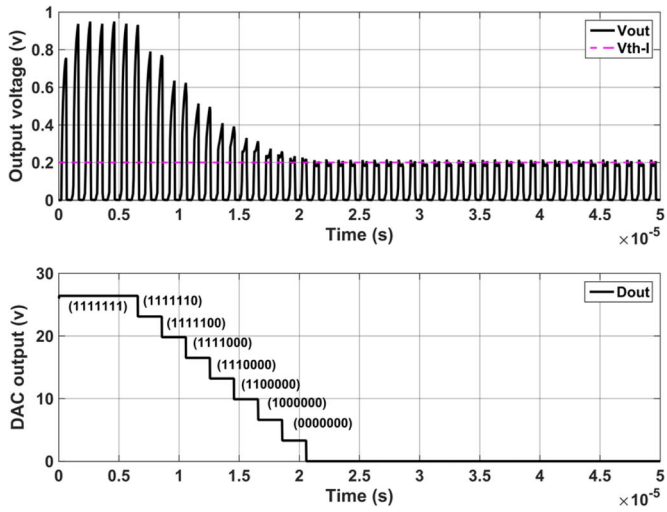

Fig. 5. Simulation results showing the calibration circuit performance.

D. Calibration Circuitry

The dynamic range of the capacitive sensor can be significantly affected by the initial value of C_S capacitors. Although the initial value is partially cancelled by the differential architecture, due to the circuit-nonidealities and current mirrors mismatch, an offset value always exists at the output voltage. To cancel this offset value, we propose a novel auto-calibration method, shown in Fig. 4(a) that can be applied for each individual pixel in the array. In each comparator's clock period, $V_{\rm out}$ is compared with two threshold voltages ($V_{{\rm th}-l}$ and $V_{{\rm th}-h}$) that determine the upper and lower limits of output voltage, respectively. If $V_{\rm out}$ is smaller than $V_{{\rm th}-l}$, the comparator produces a digital value "1," which leads to a "1" in shift register's first output bit. The shift register's outputs are connected to a latched DAC [Fig. 4(b)], once a switch is activated, a current will be added to the total current charging $C_{{\rm int}+}$ at the output node. This process will continue until $V_{\rm out}$ reaches the higher threshold value, where there will be no changes in the current sources and the total charging current will be fixed until the end of calibration phase. In an opposite scenario, if $V_{\rm out}$ becomes higher than the upper threshold voltage $(V_{{\rm th}-h})$ the discharging current will be added to the output node using latched DAC. This process repeats for all 8 channels in a single row and the calibration circuit is attached to each pixel by a 3 × 8 decoder. At the end of calibration phase, the calibration circuit is separated from the core circuit and the states of current mirrors is stored on the corresponding shift registers connected to each individual pixel. Fig. 5 shows the performance of calibration circuit while adjusting the output voltage offset. In this simulation, we made a 50% mismatch between the current mirror transistors (M_6 and M_8), and the value of C_R and C_S were selected as 50 fF. Although there is no capacitance difference, due to the mismatch, there is a 1 v offset at the output. During the calibration phase, $V_{\rm out}$ is compared to $V_{{\rm th}-l}$ and the discharging current varies accordingly and results in a lower $V_{\rm out}$. At the

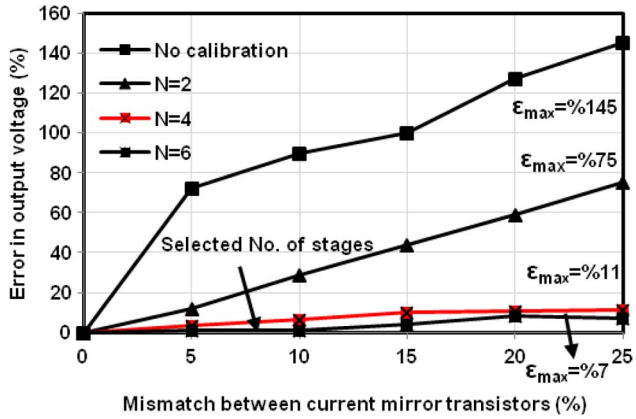

Fig. 6. Simulation results showing the effect of number of calibration stages on the total error in output voltage caused by mismatch between current mirror transistors in CBCM circuit.

end of calibration, the output voltage reaches to $V_{\mathrm{th}-l}$ value. To find the optimum number of stages for calibration circuit, we designed three different calibration circuitries with 2, 4, and 6 stages. Thereafter the aspect ratios of current mirrors in CBCM circuit was varied to create a mismatch between the transistors. The output voltage error compared to the initial point where there is no mismatch is calculated for all three calibration circuits as well as the state where no calibration circuit attached to the CBCM. The results are shown in Fig. 6. As seen, the 4 and 6 stages calibrations provide an output voltage with less than 11% error. Considering the area and power consumption, we have selected the calibration circuit design with 4-stage to compromise between accuracy and area.

III. ΣΔ Modulator Design Optimization

As previously described, by decoding the output bit-stream of ADC, the capacitance variations can be extracted. In order to study the effect of circuit's non-idealites on the overall system performance, parametric simulations can be done in circuit-level and then further decoded using an algorithm that runs in Matlab or is implemented in a FPGA platform. In order to generate a single data for the decoder algorithm, one should run the simulations for about 100 times by changing each parameters (e.g. aspect ratio of transistors or capacitances) with 1% increment or decrement. Therefore, in order to study the effect of several parameters, the required time is very significant. Additionally the required decoding time depends on the number of bits in each stream that is a function of N (number of integration cycles). Considering above mentioned issues, in order to optimize the circuit parameters, we propose a circuit behavioral model in Matlab as discussed as follows. The proposed model has the advantage of being simpler and potentially running faster compared to Spectre simulations, allowing to run multiple parametric simulations at the same time. The fundamental equation for ΣΔ modulator relating $y(n)$ to $y(n-1)$ can be described as

$$Y(n) = Y(n-1) + X(n) - Q(n) \tag{6}$$

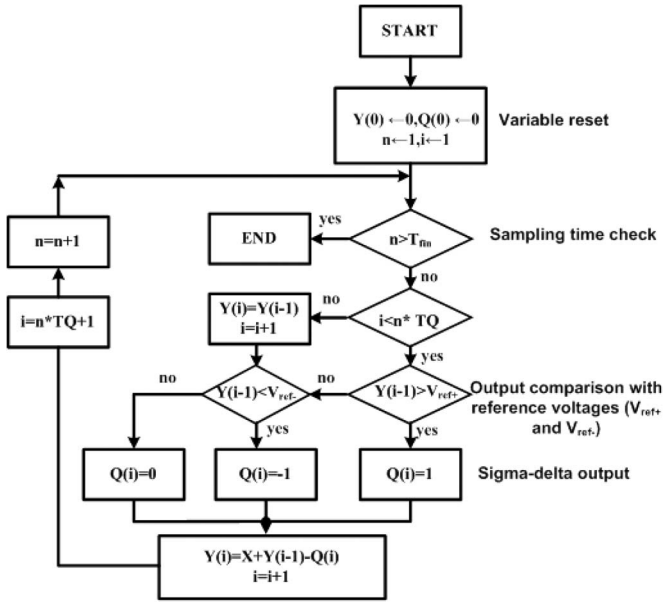

Fig. 7. Behavioral model algorithm developed in Matlab. $Y(n)$ is the output voltage, X is the constant input coming from sensing electrodes, $Q(n)$ is the output of the quantizer for nth input sample, TQ is the sampling period, and T_{fin} is total sampling time.

where $y(n)$ is the output of summing node ($V_{\mathrm{out}+}$ and $V_{\mathrm{out}-}$), $x(n)$ is the constant input (the output voltage variations which results in from $I_{\mathrm{sen}+}$ and $I_{\mathrm{sen}-}$), and $Q(n)$ is the output of the quantizer for nth input sample ($D_{\mathrm{out}+}$ and $D_{\mathrm{out}-}$). The simplified block diagram of the Matlab algorithm which is developed to describe circuit behavior is shown in Fig. 7. TQ is the sampling period (Φ_4 clock pulse) and T_{fin} is the final time of modulator operation (the number of generated bits for an input is equal to T_{fin}/TQ. According to the input value, different bit streams will be generated at the output of ΣΔ modulator. Based on this discussion, let us derive the equation for the modulator's output using the total charging current $X(n)$

$$X(n) = K\Delta C\frac{\Delta V}{\Delta t} = K\Delta C V_{\mathrm{dd}} f_s. \tag{7}$$

Assuming the digital value for $X(n)$, is represented by $Q(n)$, we have

$$Q(n) = K\Delta C\frac{\Delta V}{\Delta t} = K\Delta C V_{\mathrm{dd}} f_s \tag{8}$$

$$Q(n) = \begin{Bmatrix} KC_R V_{\mathrm{DD}} f_s & Y(n-1) > V_{\mathrm{ref}+} - V_{\mathrm{ref}-} \\ 0 & Y(n-1) \le V_{\mathrm{ref}+} - V_{\mathrm{ref}-} \end{Bmatrix}. \tag{9}$$

Finally, $Y(n)$ can be described as

$$Y(n) = Y(n-1) + \frac{TQ}{C_{\mathrm{int}}}\left[K\Delta C V_{\mathrm{DD}} f_s - Q(n)\right]. \tag{10}$$

The above equation is used for building up our model. In order to optimize the performance of the proposed modulator, we investigate the effect of critical circuit parameters variations on the performance of the ΣΔ modulator. These simulations help to find the relationship between maximum number of generated codes (resolution) and modulator parameters, including variations in integrating capacitor (C_{int}), the total sampling

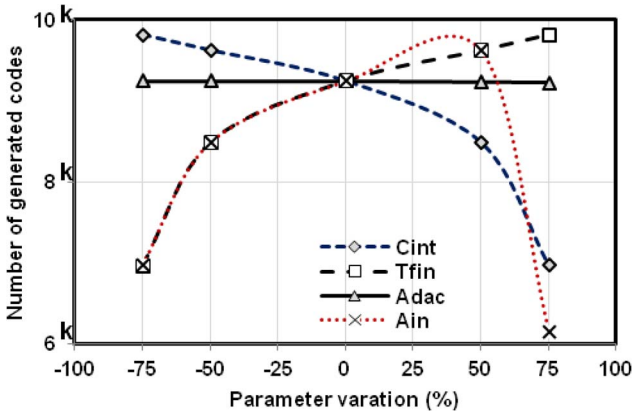

Fig. 8. Search for optimal parameter using behavioral model. Cint is integrating capacitor at CBCM output, Gin is input signal amplification factor (the gain of CBCM current mirrors), Tfin is the total sampling time that reflects the number of stored bits and Gdac is the amplification factor of DAC in modulator loop.

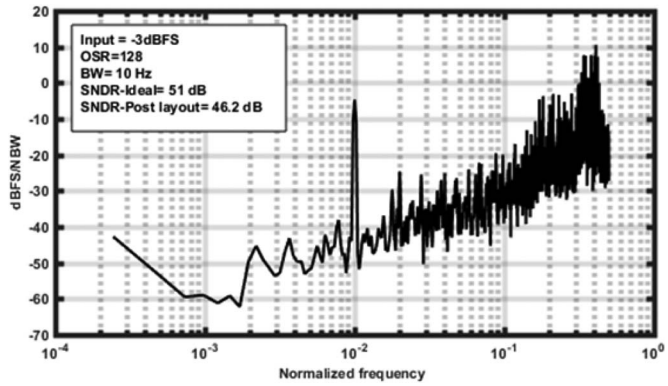

Fig. 9. Post layout simulation results: FFT waveform for the DC-input modulator with OSR $= 128$ and sampling frequency of 1 kHz.

time for a fixed comparators clock frequency $(T_{\rm fin})$, the gain of the digital to analog converter $(G_{\rm dac})$, and the gain of input signal $(G_{\rm in})$. Each parameter is varied between -75% to +75%. In each run, the number of generated codes is calculated using a Matlab algorithm. The resulting curve showing of parameters is shown in Fig. 8 and the effect of these variation is elaborated as follows.

- ***The total sampling time*** $(T_{\rm fin})$
  As shown in Fig. 8, the resolution of the modulator strongly depends on the total sampling time. The oversampling ratio (N) is calculated as the ratio of total sampling time to comparators clock $(T_{\rm fin}/TQ)$. As the simulation time and hence the number of generated bits for a constant input increases, the resolution will also increase.
- ***The input gain*** $(A_{\rm in})$
  According to (4) and (5), the analog sensitivity has a linear relationship with the current mirror gain; as the gain of the circuit increases, the variation of the output voltage for a specific charge value will increase. Although the increase in gain improves the sensitivity, but it decreases the dynamic range of modulator. For a 75% change in gain $(K = 16)$ it can be seen that the number of generated codes decreases. It is due to the fact that for a high value of the input gain, the input voltage will soon reach to $V_{\rm DD}$ saturation voltage hence the dynamic range will be limited.
- ***The DAC gain*** $(A_{\rm dac})$
  Changes in DAC gain do not have significant effect on the number of generated codes. The only consideration is that the value of the DAC current that will be subtracted from the total input current should be larger than the input current, otherwise the modulator will not operate properly.
- ***The integrating capacitor*** $(C_{\rm int})$
  Referring to Fig. 8, as the value of the capacitance decreases the number of generated codes increases. This can be justified using (8). The analog output sensitivity has an inverse linear relationship with the value of capacitance and reducing the value of the capacitor will increase sensitivity of the circuit and hence the resolution of the modulator. It should be mentioned that the minimum value of the capacitor is limited by the total parasitic capacitances at the output node. After optimizing the circuit performance using Matlab model, the parameters are used to re-design the circuit.

After optimization procedure, we performed noise-analyses on the DC-input modulator to determine the effective number of bits (ENOB) and resolution. Theoretically, The signal to noise ratio for an oversampled ADC is obtained by [18]

$$\text{SNDR} = 3.01 - n(2\,\text{L} + 1) - 9.36\,\text{L} - 2.76 \qquad (11)$$

where OSR $= 2^n$ and L is modulator's order. Using above formula, the maximum value for SNDR for a 1st order $\Sigma\Delta$ modulator with OSR $= 128$ is 51 dB which is equal to 8.25 bits resolution. The post layout simulation results for proposed $\Sigma\Delta$ modulator is shown in Fig. 9. In this figure the modulator is measured as an standalone block and it is detached from the CBCM part. A sinusoidal waveform with a very low frequency of 10 Hz (close to DC value) is used as the input. Fig. 9 shows the 4096-point FFT spectrum of a 10 Hz input signal with 1 kHz sampling frequency. The measurement bandwidth is 20 Hz and the oversampling ratio (OSR) is chosen as 128. The -20 dB/dec noise shaping can be seen in the FFT spectrum of output bitstream which confirms the performance of the 1st-order $\Sigma\Delta$ modulator. The peak SNDR with a -3 dBFS input is 46.2 dB which equals to ENOB of 7.4 bits. To investigate the effect of input variations on the noise shaping performance, the measurements are done for two input signals with 0 and 0.5 Hz frequencies and with amplitudes varying from $V_{\rm FS}$ (full-scale voltage) to -60 dB below full scale input. The results are plotted in Fig. 10(a). After validating $\Sigma\Delta$ performance as a standalone block, modulator is connected back to the CBCM and the SNDR measurements are done with varying the sensing capacitance's value as the input signal. The input capacitance is changed between 1 to 10 aF and the output bit stream was sampled at 1 kHz for 4096 points. The measured SNDR in this case is 45 dB which corresponds to the resolution of 7.2 bits. Considering the Full scale supply voltage, the minimum detectable output voltage variation with 7.2 bits is 22 mV. Since

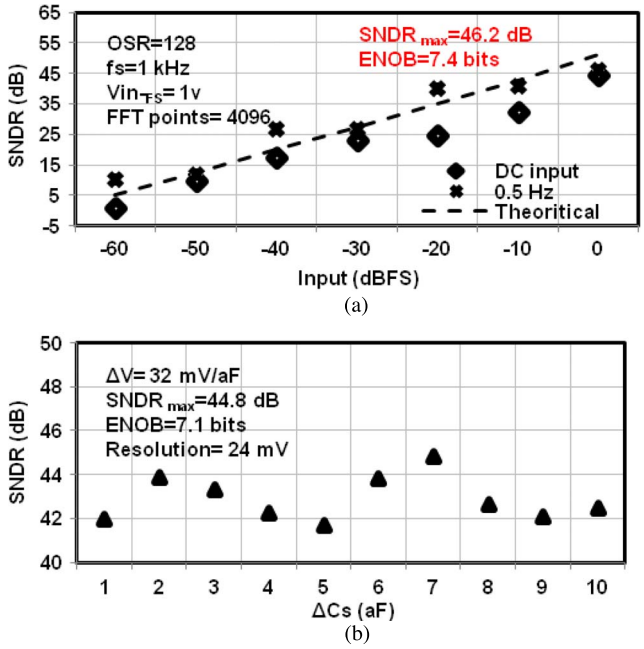

Fig. 10. Post layout simulations. (a) SNDR for two inputs with DC and 0.5 Hz frequencies and for amplitudes varying between 0 to −60 dBFS. (b) SNDR measurement for input capacitance values between 1 to 10 aF.

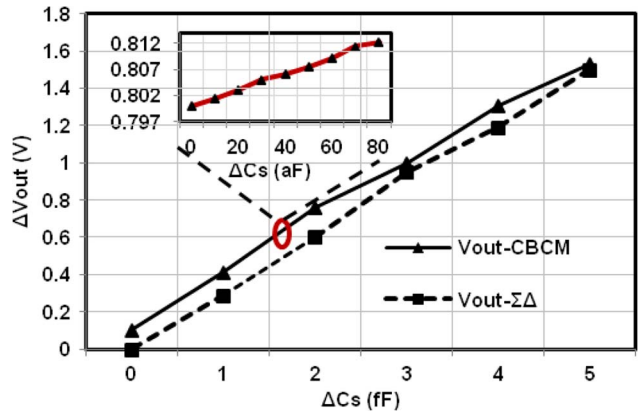

Fig. 11. Post-layout simulations: output voltage for sensing capacitance variations between 0 to 6 fF and 0 to 100 aF.

the sensitivity of CBCM circuitry is designed at 320 mV/fF, for 10 aF variations, we have 32 mV changes in the output voltage, which is more than the minimum detectable value by ΣΔ modulator. In other words the capacitance variations less than 10 aF can be detected with the modulator. To validate the resolution of proposed circuit, post-layout simulations were performed where the input capacitance is varied between 0 to 6 fF and between 0 to 100 aF. The analog output coming from CBCM and digital output of ΣΔ modulator are plotted in Fig. 11. As shown in this figure, the readout circuitry allows the detection of small capacitance values of as low as 10 aF.

IV. Experimental Results

This section demonstrate and discuses the chip fabrication and packaging, test setup and results. We show the experimental

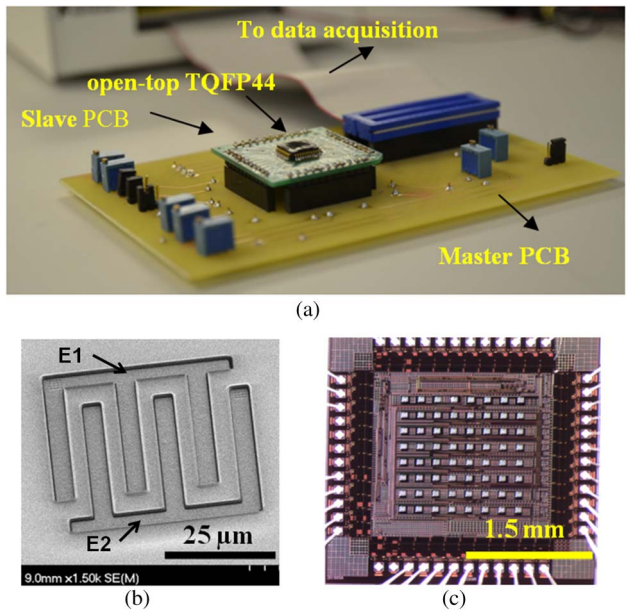

Fig. 12. Test setup and die images. (a) Assembled devices on PCB. (b) SEM image of interdigitated electrodes, two pairs of interdigitated electrodes are shown as E1 and E2. (c) Die microphotograph.

results of the fabricated chip and validate its functionality using three approaches. At the first step, we show the chip characterisation results in response to various organic solvent and then we expose the chip to different concentration of polystyrene beads with the same dielectric properties as the living cells. Finally we show the response of the chip to the adherent H1299 cell lines.

A. Chip Fabrication and Measurement Setup

The proposed integrated biosensor array is fabricated using a commercial CMOS process, TSMC (Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan) that has a minimum feature size of 0.35 μm and operates at a nominal power-supply voltage of 3.3 V. The overall system architecture and chip photograph are shown in Fig. 12. The 3×3 mm^2 chip is comprised of a 8×8 array of sensing pixels. Each pixel contains a interdigitated capacitive electrode which is connected to a readout interface via switches controlled by digital control circuitry. As seen in Fig. 12(a), the chip is packaged and mounted on a slave PCB and the then it is connected to the main PCB where control signals are provided and output signals are recorded through a data acquisition system. There are eight analog outputs from the chip and eight digital outputs coming from the eight ΣΔ modulators. An FPGA platform is programmed through Labview FPGA module for data acquisition.

B. Data Acquisition and ΣΔ Modulator Decoding

A data acquisition is implemented using a Virtex 5 FPGA system. To maximise the sampling frequency, three DMA (Direct Memory Access) FIFOs are used. The system allows to reach a maximum sampling frequency of 450 kHz for analog signals and 100 kHz for digital signals. The reading from the

eight sensors in one column is performed simultaneously and recorded data is interlaced in the FIFOs. Signals are deinterlaced from the FIFOs, reconstructed and analysed using a specially designed standalone program made with LabView software. The amplitude measurement of each CBCM waveform is performed using a standard LabView Virtual Instrument using maximum and minimum values found in the 1 ms period. A 3-bit multiplexer is used to retrieve the digital data associated with eight different sensors in each column.

C. Chip Protection and Bio-Compatible Packaging

To protect the topmost metal layer (Al) from direct exposure to cells and biological side-effects, a very thin layer of the PDMS is spin-coated on top of the electrodes. This layer offers the advantages of biocompatibility, ease of processing, and chemical inertness. To avoid sensitivity reduction, the PDMS membrane should be as thin as possible. The final thickness of PDMS membrane depends mainly on spin coating speed, spinning duration and the ratio of PDMS parts. To reach the maximum sensitivity of the sensor, we chose PDMS thickness of less than 1 μm for our application. The two parts of PDMS are mixed in 10:1 ratio and the mixture is steered by hand for 5 minutes. Thereafter the mixture is placed under the vacuumed desiccators until all the bubbles are gone and the PDMS mixture is completely degassed. In the next step we took a very small droplet of mixture using a micropipette and pour it above the CMOS chip. Using tapes, the chip was fixed on a Petri-dish as a container and it was spin-coated at the speed of 3000 rpm for 20 minutes. Finally, the fixture is placed in the oven at 80 °C to cure the PDMS membrane. The required spinning time and speed to reach the desired thickness was extracted from the data provided in [19]. Following PDMS deposition, a bio-compatible, high temperature epoxy resin (EPOTEK-353) was used to protect the bonding wires and electrical connections from biological solutions. A small plastic ring is adhered on top of the packaged chip, as a micro-well, for containing the cell culture medium. To test the bio-compatibility of epoxy resin, a simple test was done where several cell culture dishes were coated with the epoxy and the cell viability was optically observed for 2 days. The results confirmed the bio-compatibility of the selected epoxy. It was essential to clean and sterilize the CMOS chip, before culturing the cells on the electrode surface. The chips were first washed with Isopropanol (IPA) for 15 min to dissolve any possible contamination. Thereafter, they were washed with sterile distilled water and then were exposed to Ethanol for 15 min. In order to activate the surface of electrodes, they were treated in plasma cleaner for 3 min followed by 5 min UV-cleaning for sterilization. Treatment of the electrodes with plasma helps cells to attach better to the bottom of the wells. After UV sterilization all the future steps were done under the biological hood and in sterile condition.

D. Chip Calibration

To validate the calibration circuit performance, we changed the reference voltage (the input of calibration circuit) from 0 to 2 V and the response of the 64-pixels was measured at the end of calibration phase. Fig. 13 shows the calibration results were the average error in output voltage (which means the difference between final output voltage and determined reference voltages) is reported. For the sake of comparison, the

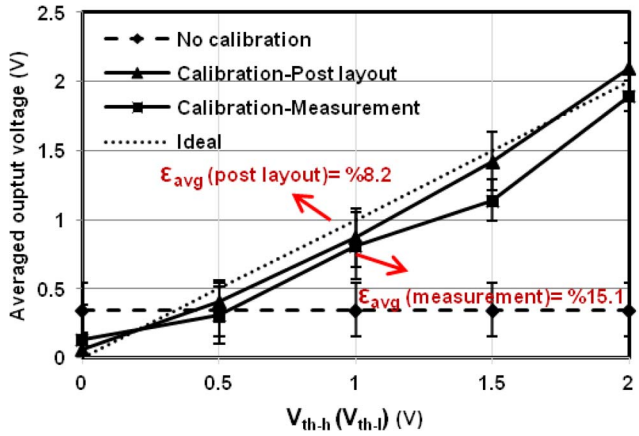

Fig. 13. Measurement results showing the performance of the calibration circuit.

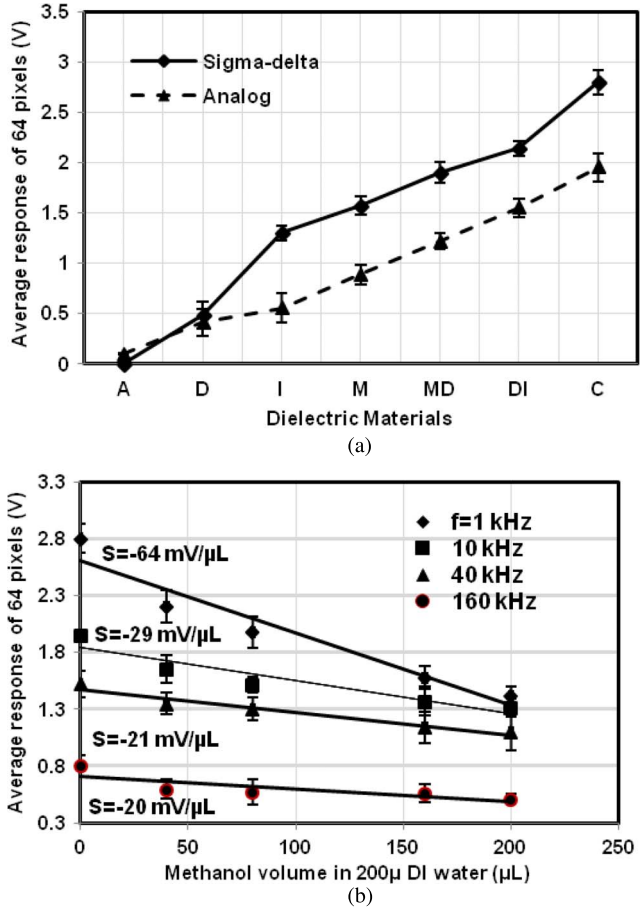

Fig. 14. Sensor response to organic solvents. (a) The average response of the 64 pixel array to various chemicals including: A: Air, D: Dischlromethane, I: Isopropanol, M: Methanol, MD: Methanol dilution, DI: Deionized water, C: Culture media. "Sigma-delta" shows the decoded value of bit-streams coming from the output of $\Sigma\Delta$ modulator and "Analog" refers to the analog output voltage at integrating capacitor's node. (b) Sensor response to the dilutions of Methanol in DI water at different working frequencies (S refers to the slope of curves).

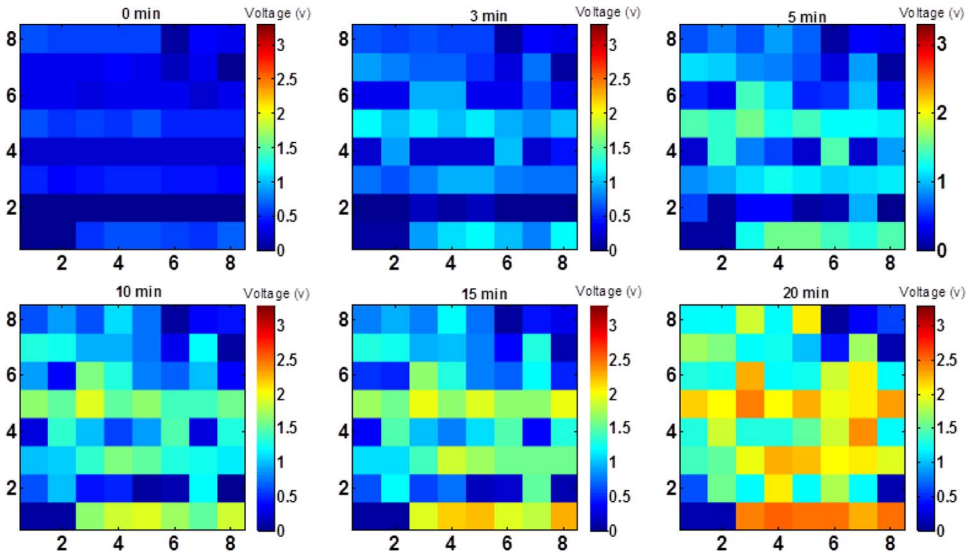

Fig. 15. Response of the chip to Polystyrene beads diluted in DI water, 1 k beads/ml concentration is shown.

post-layout simulation results and ideal curve are shown in this plot as well. The measurement confirm that the final average error for the calibration circuitry is less than 15.1%.

E. Sensor Response to Organic Solutions

To evaluate the response of the sensor to organic solvents, we introduced polar chemical solvents with different dielectric constants, namely: Isopropanol, Methanol, DI water and cell culture media which is an extremely ionic solution. Prior to test, the sensor was cleaned using DI water and then was dried on a hot plate to avoid residues remaining from the former tests. The real-time response of sensor to 200 μl of these solutions at room temperature is shown in Fig. 14(a). For the sake of comparison, the output of analog channels and also the decoded $\Sigma\Delta$ modulator bit streams are shown in the same figure. As seen, for the higher dielectric constant, the higher output voltage is achieved at the sensor's output. Although DI water and culture media have the same dielectric constants, the culture media is extremely ionic and that is why there is a noticeable variation in their responses. To show the capacitive sensor sensitivity, various dilution rates of Methanol in DI water was prepared and the real-time response of the sensor at different working frequencies was measured. The results are shown in Fig. 14(b). As the frequency increases, the output voltage variations get smaller and sensitivity decreases, leading to a higher dynamic range. This means that by having a tunable working frequency, one would be able to compromise between the sensitivity and detection range for a particular application and the properties of the solution that is under the tests. This features makes the device capable of detecting cells with different concentrations. The results shown in Fig. 14 prove the functionality of the proposed device. As expected, for the high dielectric constant values, the higher output voltage is observed. For this reason, in Fig. 14(a), using DI water rather than Dichloromethane results in the higher average output voltage. In the other hand, as seen in Fig. 14(b), the higher percentage of Methanol, results in a lower dielectric properties in comparison with the dielectric constant of DI water, and consequently a lower output voltage is observed.

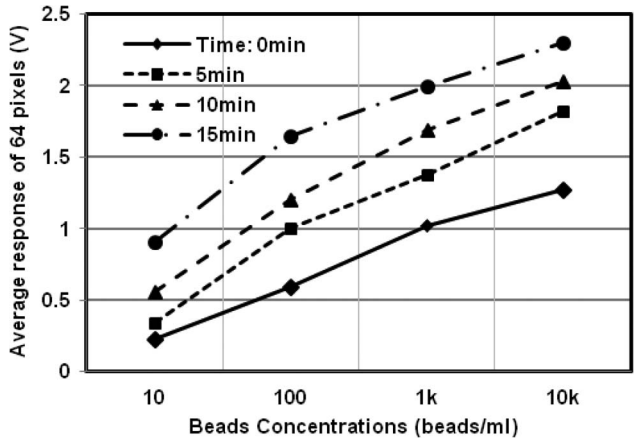

Fig. 16. Response of the chip to Polystyrene beads diluted in DI water, from 10 k beads/ml to 10 beads/ml dilutions are shown.

F. Polystyrene Beads Response

In the next step, we exposed the chip to the various concentrations of Polystyrene beads diluted in DI water. Polystyrene microparticles are negative charge stabilized colloidal particles with approximately the same electrical properties as living cells [20]. The average diameter of the beads were 10 μm. Various samples with different dilution rates were prepared ranging from 10 beads/ml to 10 k beads/ml and the response of the chip to each solution was monitored for 20 min. At the beginning of the experiment, the particles were suspended in the water but as the time passed by, more number of beads were deposited on the electrodes which resulted in an increase in the output voltage of the sensors. The response of the individual pixels to the 1 k beads/ml concentration is shown in Fig. 15.

The average output of device with 64 pixels using four different dilutions is shown in Fig. 16. At the end of 20 min no significant change was further seen and the system reached

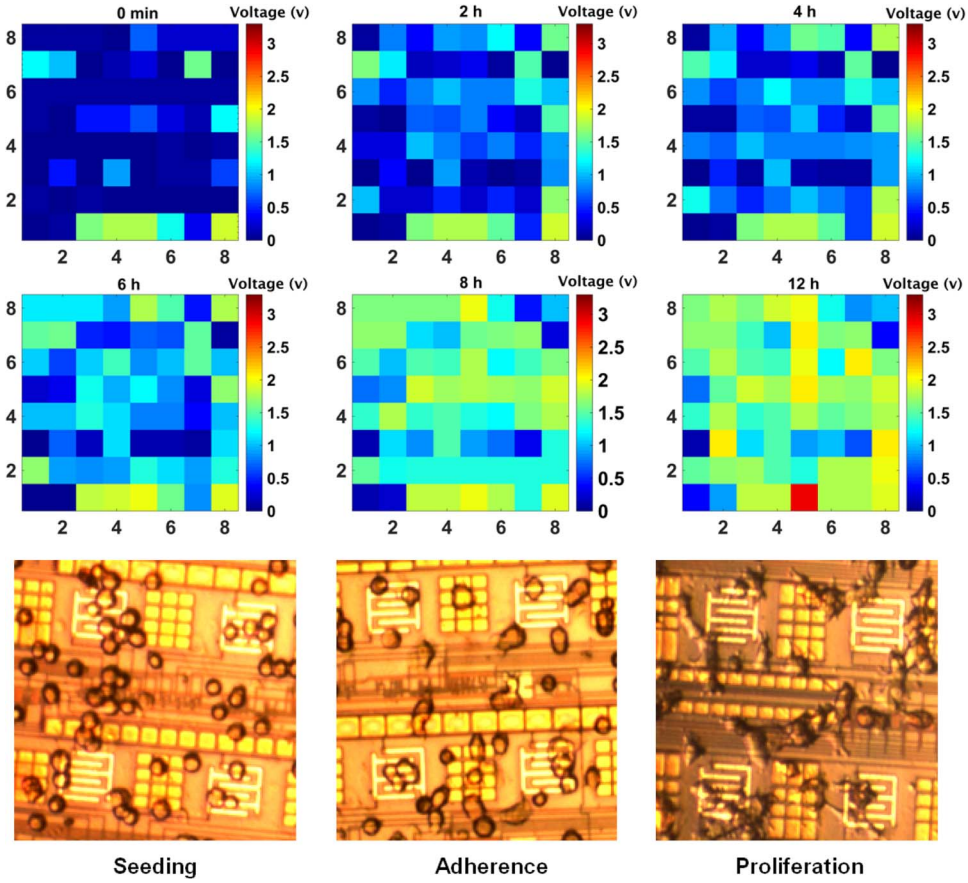

Fig. 17. CMOS chip response to 100 k cells/ml for 12 h.

to an stability. It is worth mentioning that after each step, the chip surface was thoroughly rinsed with DI water and sodium dodecyl sulfate surfactant (SDS) to remove the remaining residues of the beads over electrodes. These residues could potentially lead to an measurement error. All the experiments were carried out in the triplicates and the average values are reported. Fig. 10 shows the functionality of all 64 sensors. Each color approximately represent the number of beads on the electrode. This is due to the fact that the higher number of beads, results in a higher dielectric constant in the proximity of the sensors. As the beads randomly distribute over the chip, any set of colors can be expected. This low complexity test not only show the functionality of the proposed system, but also it might be used in other applications such as microfluidics and dynamic studies of the beads in liquids.

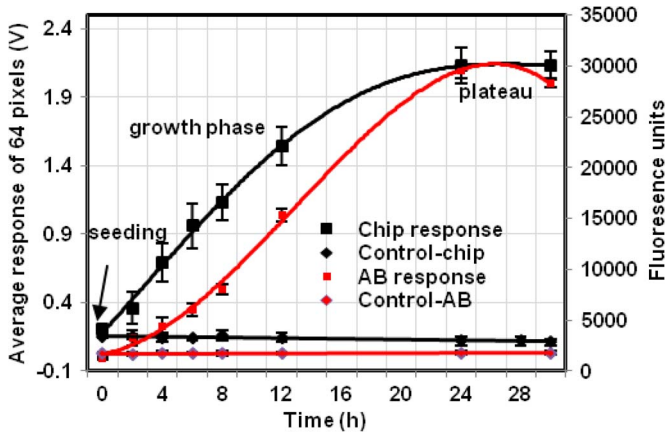

Fig. 18. Comparison of the CMOS chip results and alamarBlue results for the same concentration of the cells.

G. Cell Culture Results

A human lung carcinoma cell line, namely H1299, was chosen for the growth monitoring. The cells were first grown to confluent in RPMI medium. After two days the cell layers were rinsed with phosphate-buffered saline (PBS) with pH 7.4 (Sigma Aldrich). Then, trypsin-EDTA solution (0.25% trypsin and 1 mM EDTA; Sigma Aldrich) was used to detach the cells and RPMI Medium with 10% fetal bovine serum (FBS) was supplemented to the dispersed cell layer. The cell cultures were maintained at 37 °C under 5% CO_2 in incubator. Based on the well size on the CMOS chip, appropriate aliquots of the cell suspension were diluted to the concentration of 100 kcells/ml. Then 200 μl of cell suspension in the media was transferred to the well on top of the CMOS chips. The cell number was counted using Scepter 2.0 Digital Cell Counter (Milipore). To avoid contamination, the readout platform and associated interface circuit was placed under the biological hood during the measurements. Four CMOS chips were tested and each CMOS chip was monitored for 24 hours, and the data were sampled every 2 hour.

TABLE I
COMPARISON OF THE PROPOSED CAPACITIVE BIOSENSOR ARRAY WITH THE STATE-OF-ART

Ref.	Application	Method	Tech. (μm)	No.Electrodes	Sensing layer	ADC	Resolution
[3]	Cell proliferation monitoring	Charge-sharing	0.35	16	Si3N4	No	200mv/fF
[7]	Bacteria growth monitoring	CBCM	0.18	3	Aluminum	Sigma-delta	250 mV/fF (6bits)
[20]	Cell manipulation	Electrophoresis	0.35	32x32	Gold	No	NA
[21]	Neurotransmitter dopamine	Capacitance to frequency conversion	0.35	5x5	Sio2	No	1 fM
[22]	Bacteria detection	Capacitance to frequency conversion	0.25	16x16	Al2O3	No	55 mv/fF (37 dB)
This work	Cell growth monitoring	CBCM	0.35	64	Aluminum +PDMS	Sigma-delta (8-channel)	350 mV/fF (46 dB)

Fig. 17 shows the response of the chip to the 100 k cells/ml dilution over 12 hours. As demonstrated in this figure, in first 4 hours before cell adhesion to the electrodes, there is a small increase in the value of output voltage. As cells attach to the electrode, and start spreading over the electrode surface, the output voltage increases accordingly. Since the partial evaporation of media can affect the measurement accuracy, a loose cap was used on top of the well which provides gas exchange between cells and incubator environment and at the same time protects the media from evaporation. Moreover, due to the high humidity of incubator, the effect of evaporation is negligible and can be discounted in the measurements. To validate the chip results with a standard cell assay, alamarBlue was used. AlamarBlue is a fluorometric/colorimetric growth assay that is based on the metabolic activity of the cells. The oxidation-reduction indicator in the assay fluoresces and changes color in response to the chemical reduction of growth medium resulting from cell growth. To measure the cell growth rate using alamarBlue, the cells were harvested in the log phase and then diluted to the desirable concentration (100 k cells/ml). Thereafter, 200 μl of the cell suspensions and 10 μl of alamarBlue were added to the 96-well plates. The wells were kept in incubator and the fluorescence was measured by using a spectrophotometer, every 2 h, for 24 hours. The fluorescence measurements were performed with excitation wavelength at 570 nm and emission wavelength at 600 nm. The CMOS chip results and alamarBlue readings are illustrated in a same graph in Fig. 18. It is seen that after 8 hours the cells in the chip and in the wells have entered the log (exponential) phase and there is a noticeable increase in the slope of both curves. The graph shows a consistency between two results and the chip could successfully detect two phases (lag and log) in cell growth curve. Comparing these results with the results of our first prototype, shown in Fig. 1(c), confirm the success of the new capacitive sensor array in cell growth detection and cell screening application. As the continuation of this work, we are working towards the implementation of a high-throughput microfluidic structure to study the cells in micro-wells individually. A summary of proposed capacitive biosensor specifications as well as its comparison with the state-of-art is provided in Table I.

V. CONCLUSION

In this paper we presented an 8×8 capacitive sensor array for cell growth monitoring. The proposed device consists of 64 interdigitated electrodes fabricated in topmost metal layer of 0.35 μm CMOS technology. Each row of eight electrodes is connected to a core-CBCM capacitance to voltage converter incorporated with a DC-input $\Sigma\Delta$ modulator. We demonstrated the device functionality using various organic solvents with different dielectric constants. Moreover, the response of the sensing chip to polystyrene beads which have the same dimension and electrical properties as living cells are shown. Thanks to the high sensitivity of readout interface, the chip is able to detect the presence of single beads on the electrodes. Due to the design simplicity and compactness, the platform can be used as an efficient tool for cell monitoring purposes. The experimental results including the cell culture results on each single electrode of 64-electrodes array demonstrate the applicability of the proposed device for high-throughput screening of cellular activities suitable for a variety of life science applications such as drug discovery.

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