DC-100 kHz Tunable Readout IC for Impedance Spectroscopy and Amperometric Measurement of Electrochemical Sensors

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***Abstract*—This paper presents a low-noise, front-end sensor IC that includes both AC impedance spectroscopy and DC amperometric measurement capabilities for electrochemical and biosensor applications. A common-gate current buffer topology is proposed that supports both current-mode and voltage-mode sensor signals to allow an input frequency range from DC to 100 kHz. Low-noise operation is achieved across a wide input frequency range using tunable high-pass and low-pass frequency response. In addition, an incremental delta-sigma modulator with embedded frequency response analysis serves as both on-chip impedance analyzer and current-driven analog-to-digital converter. Implemented using a 0.18 µm CMOS process, this work achieves 45 fA/$\sqrt{\text{Hz}}$ input current noise density at 1 kHz. Input dynamic range exceeding 80 dB is achieved up to 10 kHz bandwidth, with a maximum of 104 dB dynamic range at 10 Hz.**

I. Introduction

Electrochemical sensing is increasingly used for measurements in chemical and biomedical applications, including non-invasive monitoring, DNA detection, and cell characterization [1]–[3]. As is depicted in Fig. 1, a variety of methods exist to extract information from an electrode-electrolyte interface, which can be categorized by the applied stimulation (constant or sinusoidal) and the measured electrical quantity (voltage, current, or impedance); each approach requires different readout circuits. For example, cyclic voltammetry (CV) employs a voltage ramp excitation, and a resulting current is measured. For electrochemical impedance spectroscopy (EIS), sinusoidal voltage (current) is applied, and the corresponding current (voltage) is measured to calculate the characteristic impedance of the sensor. As such, a multi-functional sensor interface circuit requires both wide input range and bandwidth selection.

CMOS-integrated EIS interfaces have been previously demonstrated with low-noise performance and wide input frequency range for biosensor applications, but these mixer-based architectures are unable to support very low frequency or DC amperometric sensing [1], [4]. A multi-functional system-on-chip (SoC) including both amperometric readout and impedance measurement was demonstrated in [3], however separate circuitry was used for each readout mode supporting different amplitude and frequency ranges, increasing both design complexity and power consumption. Such approaches have not demonstrated circuit re-use to support both operational modes using a combined, reconfigurable architecture.

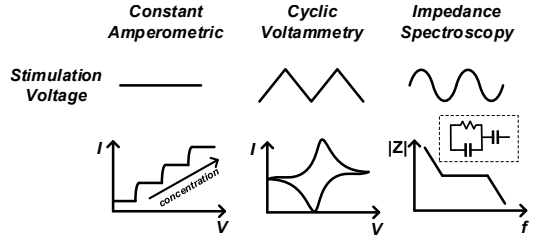

Fig. 1. Stimulation electrode voltage and resulting response of three electroanalytical methods with amperometric readout.

In this work, we propose an integrated readout architecture that is reconfigurable to perform both general amperometric sensing and impedance analysis. A new common-gate current buffer with adjustable high-pass and low-pass corner frequencies is introduced to filter noise from outside the targeted frequency band, programmable for different input frequencies. An incremental delta-sigma modulator is designed to perform complex impedance extraction and signal digitization using the same circuitry. A complete current-to-digital sensor front-end interface is implemented in a 0.18 µm CMOS process, and measured results demonstrate low noise across wide input frequency range. The approach enables true DC to 100 kHz measurement to support EIS, CV, and amperometry.

II. System Design

Figure 2a shows the overall architecture of the proposed front-end interface for electrochemical sensors, including a current conveyor with selectable bandwidth, current and voltage gain stages for both operating modes, low-pass filter, and incremental delta-sigma modulator for electrochemical impedance analysis or amperometric digitization.

A. Proposed Current Buffer

A schematic of the proposed current buffer circuit is shown in Fig. 2b. Unlike a current mirror used in conventional current conveyors, a coupling capacitor C_C is used for current conduction. By designing C_C sufficiently larger than parasitic capacitances, all AC current will flow through C_C to a low-impedance stage, which effectively adds a high-pass feature to the current transfer function, eliminating DC offset and reducing undesired low-frequency noise.

A unity-gain-feedback transconductance stage G_{ML} is added as the current buffer load to define and control the DC gain

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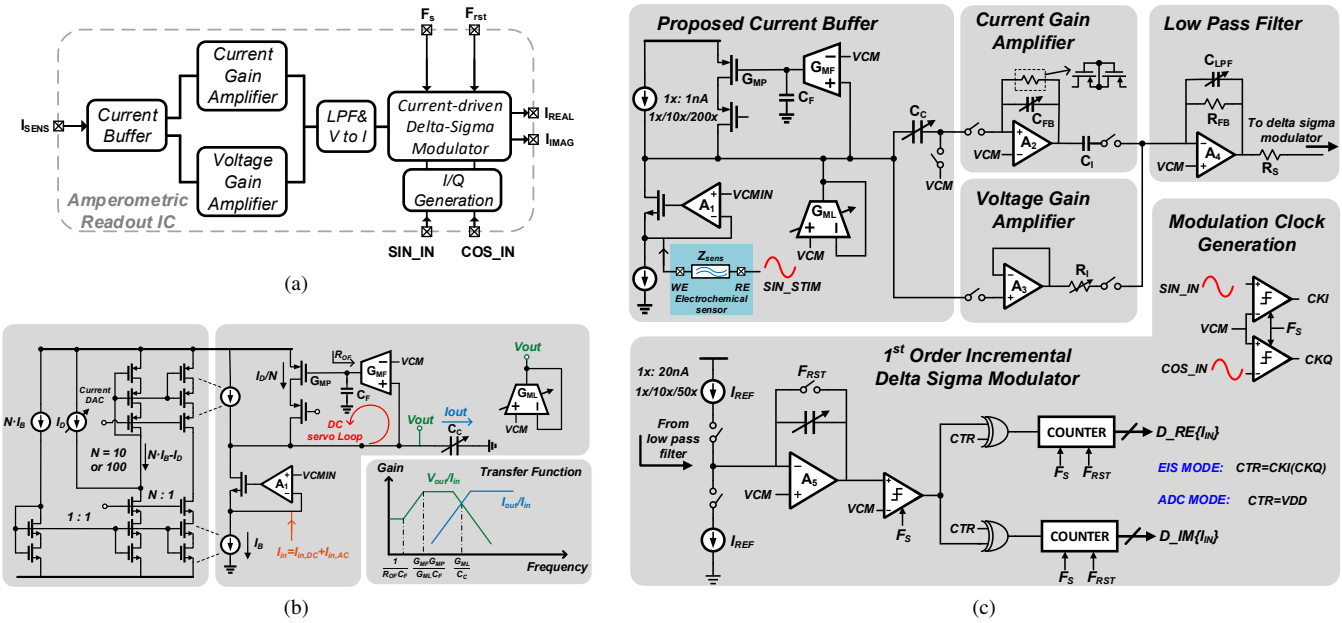

(a) (b) (c)

Fig. 2. (a) Architectural level block diagram, (b) implementation details of proposed current buffer, and (c) block diagram of proposed amperometric sensing interface readout IC for electrochemical sensors.

(equal to $1/G_{ML}$). To reduce the noise contribution from G_{ML}, a small G_{ML} value should be used, resulting in a large DC gain of the current buffer. For many biosensor and electrochemical applications, where leakage current may be in the nanoampere range, this may degrade stability of the DC operating point and reduce the dynamic range. Additionally, applications such as EIS measure only a specific frequency range of AC current. Therefore, a DC servo loop with an inverting low-pass filter is added, and difference current provided by current source transconductance G_{MP} is summed at the V_{out} node. The transfer function for voltage gain can be derived as

$$\frac{V_{out}}{I_{in}} = \frac{1}{C_C} \frac{s + \frac{1}{R_{OF}C_F}}{s^2 + \frac{G_{ML}}{C_C}s + \frac{G_{MF}G_{MP}}{C_F C_C}}. \quad (1)$$

If pole p_1=G_{ML}/C_C can be designed to be much higher than pole p_2=$(G_{MF}G_{MP})/(G_{ML}C_F)$, both high-pass and low-pass behaviors can be obtained for the voltage gain transfer function, as is shown in Fig. 2b. For the current gain transfer function, the high-pass frequency is also set by G_{ML}/C_C, the low-pass frequency of voltage gain transfer function. Therefore, high-pass frequency tuning can added by making G_{ML} and C_C adjustable.

The high-pass frequency G_{ML}/C_C will be bounded by the largest feasible on-chip capacitor. This limits the detectable frequency range only for capacitively-coupled current I_{out}. For low input frequencies, the signal can alternatively be processed in the voltage domain, either using the feedback loop or by disabling the loop, enabling low frequency (and DC) input signals without requiring very large C_C.

In this design, C_C is designed as a 4-bit programmable capacitor bank with a maximum 15 pF total capacitance. Pole p_2 must also be tunable and sufficiently small compared to p_1, while avoiding large on-chip capacitor C_F. To achieve this aim, a difference current mirror topology is used, as shown in Fig. 2b. The effective bias current flowing through transconductance G_{MP} is equal to the current difference between the top and bottom current source, which is generated by intentionally injecting a small current I_D into the current mirror. By using a large mirroring ratio, N, 10 or 100 in this design, a small current can be obtained in the G_{MP} branch. By designing I_D as a programmable current DAC, a sub-100 pA current can be generated, including compensating mismatch current from top and bottom sources. As a result, a small programmable G_{MP} value is achieved with a C_F value of 15 pF.

A regulated, common-gate input stage is adopted both to reduce input impedance and to set the DC potential voltage for the input working electrode (WE). As implemented, the feedback amplifier A_1 consumes 1.5 µA to maintain low power and low noise below 100 kHz with tens of pF input capacitance. As the current source is the major noise contributor of the current buffer stage, the N- and P-type current sources are designed to have 1/10/200 nA biasing current to support both low-noise and high-input-current applications. Instead of chopping, which would introduce charge injection and switching noise to the sensitive working electrode, long channel length devices (15 µm) are used for the current source to reduce flicker noise. Feedback stage G_{MF} is biased at 1 nA. G_{ML} is programmable, with a minimum bias current of 1 nA and a maximum of 100 nA; maximum bias current determines the maximum input DC current in voltage mode. Both G_{MF} and G_{ML} are designed as single-stage cascode amplifiers for simplicity and low noise.

B. Gain Stage and LPF

As depicted in Fig. 2c, a variable gain stage is inserted in the signal chain following the front-end current buffer to minimize noise contributions from later stages and extend signal dynamic range. As both current and voltage domain

signals can be processed based on the input signal frequency, a gain multiplexer for both current and voltage modes is designed. For the current amplifier, a capacitive programmable gain amplifier (PGA) is implemented using a pseudo-resistor to define the DC operating path. The current gain is set by C_I/C_{FB}. As designed, C_I is 10 pF, and C_{FB} is a programmable capacitor with a minimum value of 200 fF, for a maximum current gain of 50. The current gain stage can also be bypassed (switch not shown) for processing large input signal current.

The voltage gain amplifier is formed by a unity-gain buffer, A_3, followed by a inverting amplifier A_4 with feedback resistance R_{FB}. A_3 provides a large input impedance, such that the output impedance of node V_{out} is unaltered. Voltage gain is determined by the ratio between R_{FB} (1 MΩ) and R_I. In this design, the ratio is designed as 1 or 5. Variable voltage gain can also be provided by adjustable G_{ML} in the first stage.

Amplifier A_4 with R_{FB} also serves as a transimpedance amplifier (TIA) for the output from the current amplifier, which is converted to the voltage. A programmable capacitor, C_{LPF}, is added in parallel to R_{FB} to provide a variable low-pass characteristic. $A_2 - A_4$ are all implemented as two-stage, folded-cascode amplifiers. A_2 and A_3 each consume 6 µA, and A_4 consumes 12 µA. The voltage signal at the output of the LPF is converted back to current by resistor R_S for subsequent current-driven delta-sigma modulator. R_S is designed identically to R_{FB} for good matching.

C. Delta-Sigma Impedance Analyzer

While delta-sigma-based impedance analyzers have been previously demonstrated [5], [6], in this work, the frequency response analysis algorithm is embedded directly in an incremental delta-sigma modulator. As shown in Fig. 2c, a reset signal is added to clear all memory elements, which provides sample-by-sample conversion. Moreover, by moving the modulation signal CKI and CKQ from analog domain to digital domain using an XOR gate [7], the modulator can be easily reconfigured for amperometry and impedance analysis modes. If no modulation signal is applied, the modulator operates as a simple ADC with a Nyquist rate of F_{RST}, digitizing the input current signal. If a modulation signal is applied and F_{RST} is set equal to the input signal frequency, the modulator performs impedance analysis to obtain digitized real and imaginary components of the input signal. The relationship between output and real (imaginary) input component is

$$I_{RE(IM)} = \frac{2}{\pi}\frac{D_{RE(IM)}I_{REF}}{OSR} \quad (2)$$

where OSR is the ratio between oversampling frequency F_S and reset frequency F_{RST}. The maximum F_S is chosen as 15 MHz to achieve sufficient resolution for 100 KHz input. A programmable current DAC with 20 nA/200 nA/1 uA current is designed to support a wide input signal range. A programmable integrating capacitor with minimum 50 fF and maximum 7.5 pF capacitance also enables a wide range of input currents and F_S values. The modulation signals CKI and CKQ are generated by comparator from SIN_IN and COS_IN and synchronized with input stimulation signal SIN_STIM.

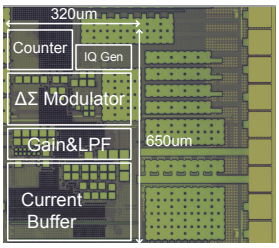

Fig. 3. Die photo of fabricated EIS and amperometric measurement IC.

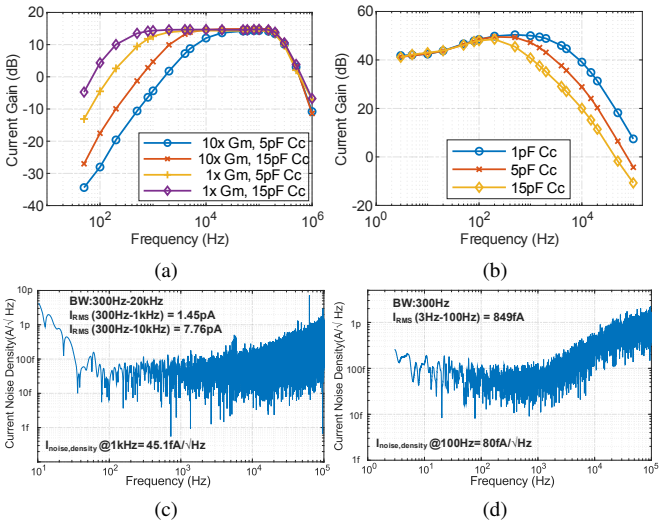

Fig. 4. Measured tunable current gain transfer function for (a) current mode and (b) voltage mode for different values of G_m and C_C, and mesaured input-referred current noise density of front-end circuit in (b) current mode and (c) voltage mode for 1 nA bias current with 2 pF input capacitance

III. Measurement Results

The design was fabricated in a general purpose 0.18 µm CMOS process and occupies $320 \times 650\,\mu m^2$; a die photo is shown in Fig. 3. Standalone copies of analog front-end circuits were included to characterize individual block performance.

Figures 4a and 4b show the measured overall current gain transfer function for both current and voltage modes. In current mode, current gain was set to 5, and G_m and C_C enable programmable high-pass corner frequencies. In voltage mode, G_m was set to an equivalent current gain of ∼300.

The noise performance of the front-end circuit in both current mode and voltage mode was measured, as shown in Figs. 4c and 4d. For current mode, current gain was set to 50 and high-pass corner frequency was set to 300 Hz. The input-referred current noise PSD at 1 kHz is 45.1fA/√Hz, which gives 1.45 pA RMS current noise for 1 kHz bandwidth. For voltage mode, 300 Hz bandwidth with equivalent current gain of 420 was set. 80 fA/√Hz current PSD at 100 Hz and 849 fA RMS current are achieved. The bias current for the current buffer was set to 1 nA for minimum noise in both modes.

The complete readout IC combining analog front-end and delta-sigma modulator was also measured. With the modulator in EIS mode, the magnitude of real and imaginary digital output codes were obtained for varying input frequency; Fig. 5 summarizes measured output magnitude codes versus input sinusoid amplitude. Voltage and current modes were operated

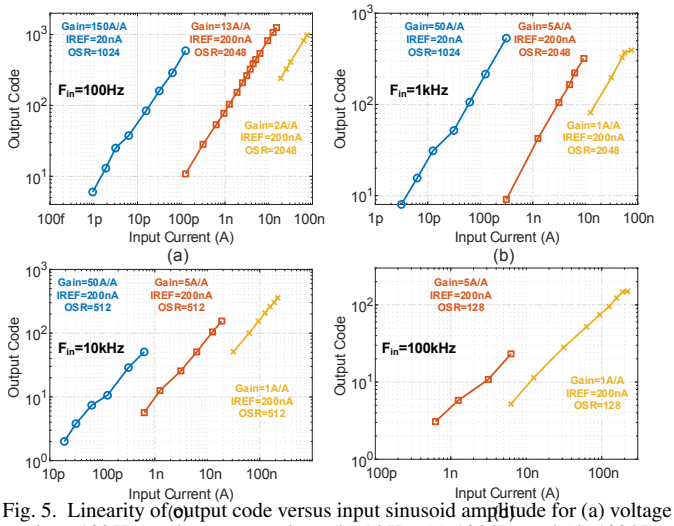

Fig. 5. Linearity of output code versus input sinusoid amplitude for (a) voltage mode at 100 Hz, and current mode at (b) 1 kHz, (c) 10 kHz, and (d) 100 kHz.

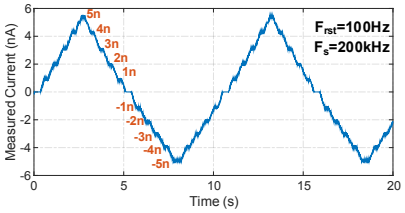

Fig. 6. Transient waveform of measured ADC output with a swept, quasi-static DC current input using a source meter (Keithley 2450).

for 100 Hz and for 1, 10, 100 kHz, respectively. Minimum detectable signal level is higher than would be expected from only front-end RMS noise and is limited by quantization noise. More than 80 dB dynamic range is achieved up to 10 kHz, with a maximum of 104 dB dynamic range at 10 Hz.

An input DC current sweep was performed using source meter to demonstrate the amperometric measurement capability of the proposed readout IC. The measured transient waveform of ADC output is shown in Fig. 6, presenting a good low-current sensing capability with this work.

A discrete model cell was used to demonstrate the proposed architecture for EIS, as shown in Fig. 7a, following phase calibration. A 20 mV_{pp} sinusoidal signal was swept across

TABLE I
PERFORMANCE COMPARISON

Reference	[1]	[4]	[2]	This Work
Application	EIS	EIS	CV/CA	EIS/CV/CA
Process (µm)	0.35	0.18	0.18	0.18
Noise Floor (fA/$\sqrt{Hz}$)	-	51 (0.2nA)	46 (0.2nA)	45.1@1kHz (1nA)
RMS Noise	577pA$_{rms}$ (1kHz)	-	0.48pA$_{rms}$ (110Hz)	1.45pA$_{rms}$ (1kHz)
Frequency Range (Hz)	10-50M	10-10k	110-10k	DC-100k
Current Range	±25µA	±2µA	±50nA	±100nA*, ±200nA**
Dynamic Range(dB)	97@10Hz	152	104	104@10Hz 81@10kHz
Power Consumption	84.8mW @3.3V	144µW @1.8V	12.1µW*** @1.8V	311.4µW @1.8V
Area (mm^2)	4	0.48	0.03***	0.208

* Voltage Mode; ** Current Mode; *** ADC not included.

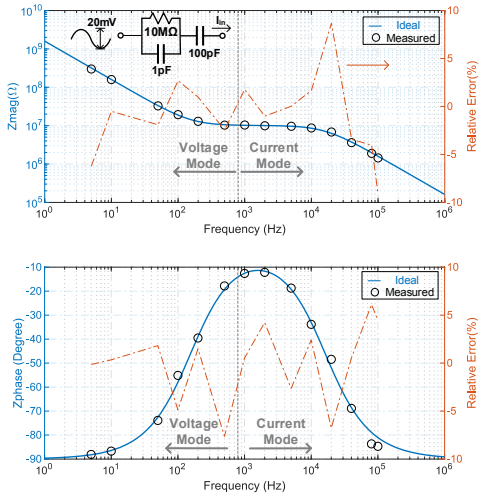

Fig. 7. Impedance spectroscopy measurements using impedance model cell: (a) magnitude response and (b) phase response, both with relative error.

frequncy as input stimulation. Impedance spectroscopy was conducted from 5 Hz to 500 Hz in voltage mode, and from 1 kHz up to 100 Hz in current mode. Measured results are shown for magnitude response in Fig. 7a and phase response in Fig. 7b compared to an ideal model. Relative error is also plotted, demonstrating $<10\%$ error across wide frequency range for high impedance measurement.

A comparison with related work is provided in Table I. Leveraging a new current buffer topology, combined voltage and current processing, and a reconfigurable delta-sigma modulator, the proposed architecture enables wide input frequency range and dynamic range for both impedance-based and amperometric electrochemical sensing.

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